

Nirvana 13 Discrete GDDR5 Schematics Document

**Sandy Bridge
Intel PCH**

2011-01-18

REV : A00

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DY :None Installed

10mW: External circuit for 10mW solution installed.

GSENSOR_ADI: Stuff for ADI G-Sensor

VCCSA_PWM: Stuff for VCCSA PWM solution.

P2800A1: Stuff for P2800EA1

<Core Design>



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Title

Cover

Size
A3

Document Number

Nirvana 13

Rev
A00

Date: Tuesday, January 18, 2011

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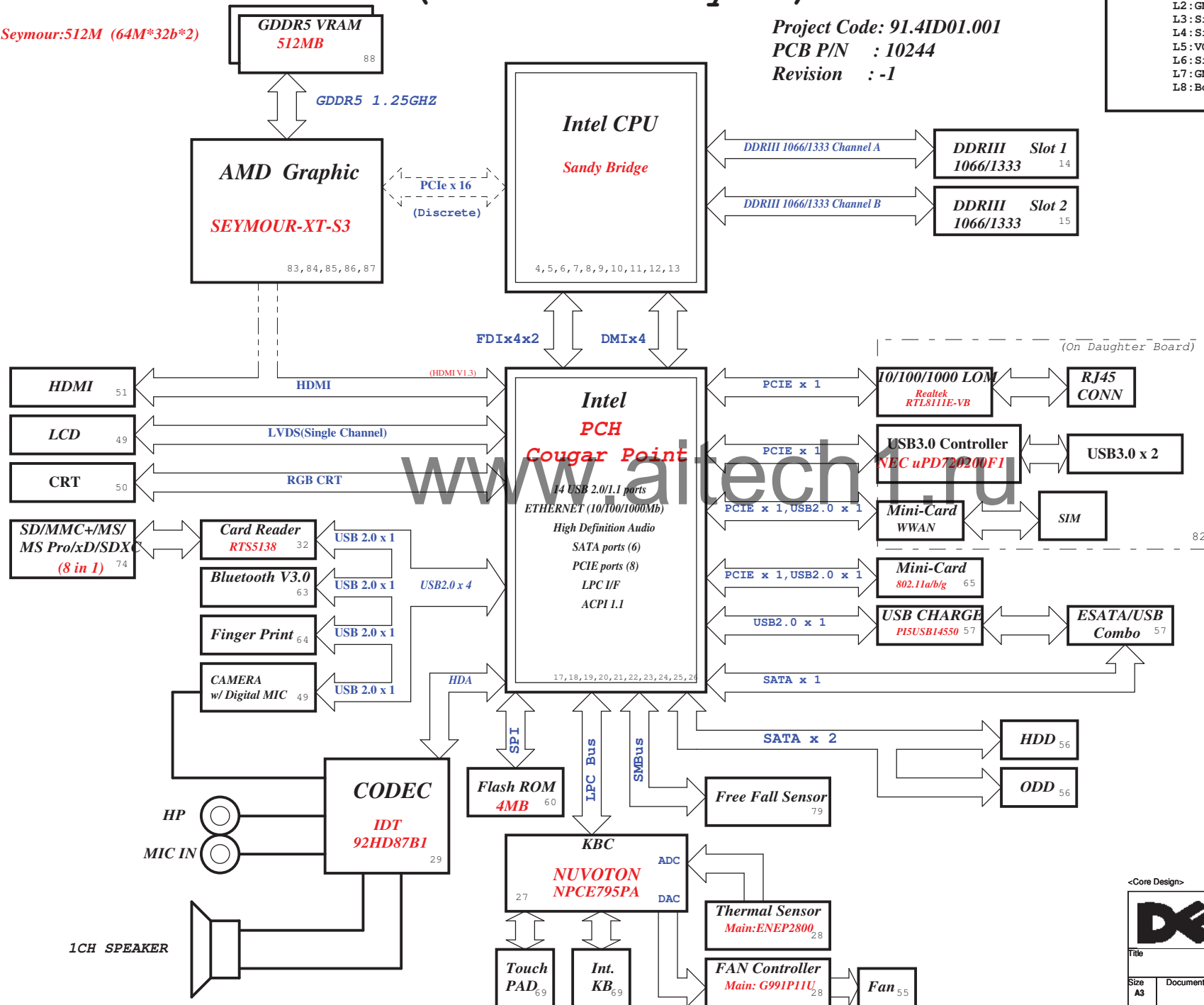
Nirvana 13 Block Diagram (Discrete 8 layers)

Seymour:512M (64M*32b*2)

Project Code: 91.4ID01.001

PCB P/N : 10244

Revision : -1



PCB LAYER		CPU DC/DC	
DIS		VT1316+VT1317 42	
L1:Top L2:GND L3:Signal L4:Signal L5:VCC L6:Signal L7:GND L8:Bottom	INPUTS		OUTPUTS
	5V_S5		VCC_CORE
	SYSTEM DC/DC		
	VT1316+VT1317 44		
	INPUTS		OUTPUTS
	5V_S5		VCC_GFXCORE
	SYSTEM DC/DC		
	TPS51461 48		
	INPUTS		OUTPUTS
	5V_S5		0D85V_S0
VGA			
VT357 92			
INPUTS		OUTPUTS	
5V_S0		VGA_CORE	
SYSTEM DC/DC			
VT358/RT9026 46			
INPUTS		OUTPUTS	
5V_S5/5V_S5		1D5V_S3 0D75V_S0 DDR_VREF_S3	
SYSTEM DC/DC			
VT357 45			
INPUTS		OUTPUTS	
5V_S5		1D05V_VTT	
TI CHARGER			
BQ24745 40			
INPUTS		OUTPUTS	
+DC_IN_S5 +PBATT		DCBATOUT	
SYSTEM DC/DC			
TPS51427 41			
INPUTS		OUTPUTS	
DCBATOUT		5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5	
SYSTEM DC/DC			
TPS51311 47			
INPUTS		OUTPUTS	
3D3V_S5		1D8V_S0	
SYSTEM DC/DC			
G9731 93			
INPUTS		OUTPUTS	
1D5V_S3		1V_VGA_S0	
Switches 36,93			
INPUTS		OUTPUTS	
1D5V_S3 5V_S5 3D3V_S5 1D8V_S0 1D5V_S3		1D5V_S0 5V_S0 3D3V_S0 1D8V_VGA_S0 1D5V_VGA_S0	

45

QNN

USB3.0 x 2

82

ATA/USB Combo 57

<Core Design>

PCB Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Enable when Pull-up.
INIT3_3V#	Weak internal pull-up. This signal should not be pulled low. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable Integrated 1.05 V VRMs is enabled when high. This signal should always be pulled high
DF_TVS	DMI and FDI Tx/Rx Termination Voltage Weak internal pull-down. It needs to be connected to PROC_SELECT with a 1K±5% pull-up resistor to PCH VCCPNAND rail and a 4.7K±5% series resistor.
SATA1GP /GPIO19	Boot BIOS Strap bit 0 This Signal has a weak internal pull-up. Note: This field determines the destination of accesses to the BIOS memory range. This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC
HDA_SDO	Signal has a weak internal pull-down. Default: the security measures defined in the Flash Descriptor will be in effect. Pull-up: the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing or debug environments ONLY.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. Needs to be pulled High for Huron River platform.
GPIO15	TLS Confidentiality Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: A strong pull-up may be needed for GPIO functionality
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable This signal enables the internal Deep Sleep 1.05 V regulators. This signal must be always pulled-up to VccRTC.
GPIO28	On-Die PLL Voltage Regulator This signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail.

PCIE Routing

LANE1	X
LANE2	LAN (I/O Board)
LANE3	Mini Card2 (WWAN)
LANE4	Mini Card1 (WLAN)
LANE5	USB3.0
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	X
1	ESATA / USB COMBO
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Processor Strapping


Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	0
CFG[4]	Display Port Presence strap	Disabled - No Physical Display Port attached to Embedded Display Port. Enabled - An external Display Port device is connected to the Embedded Display Port	1
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S5 1D5V_S3 DDR_VREF_S5	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		Ref Des	HURON RIVER ORB Address Hex Bus
Device			
EC SMBus 1 Battery Capacity Board			KBC_SDA1/KBC_SCL1 KBC_SDA1/KBC_SCL1
EC SMBus 2 PCH MXM LCD Thermal Sensor			KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
PCH SMBus CK505 Clock Generator SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

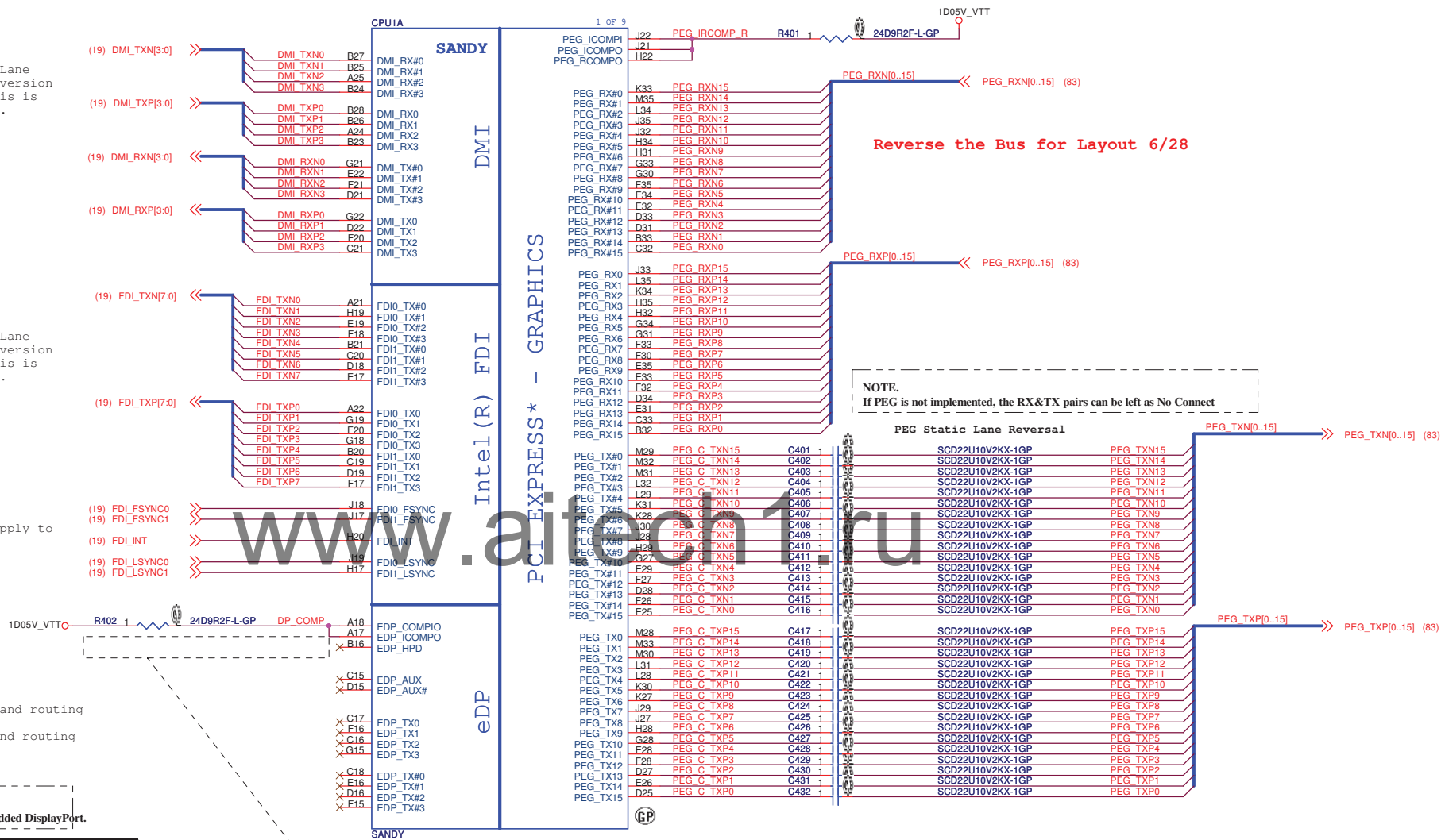
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

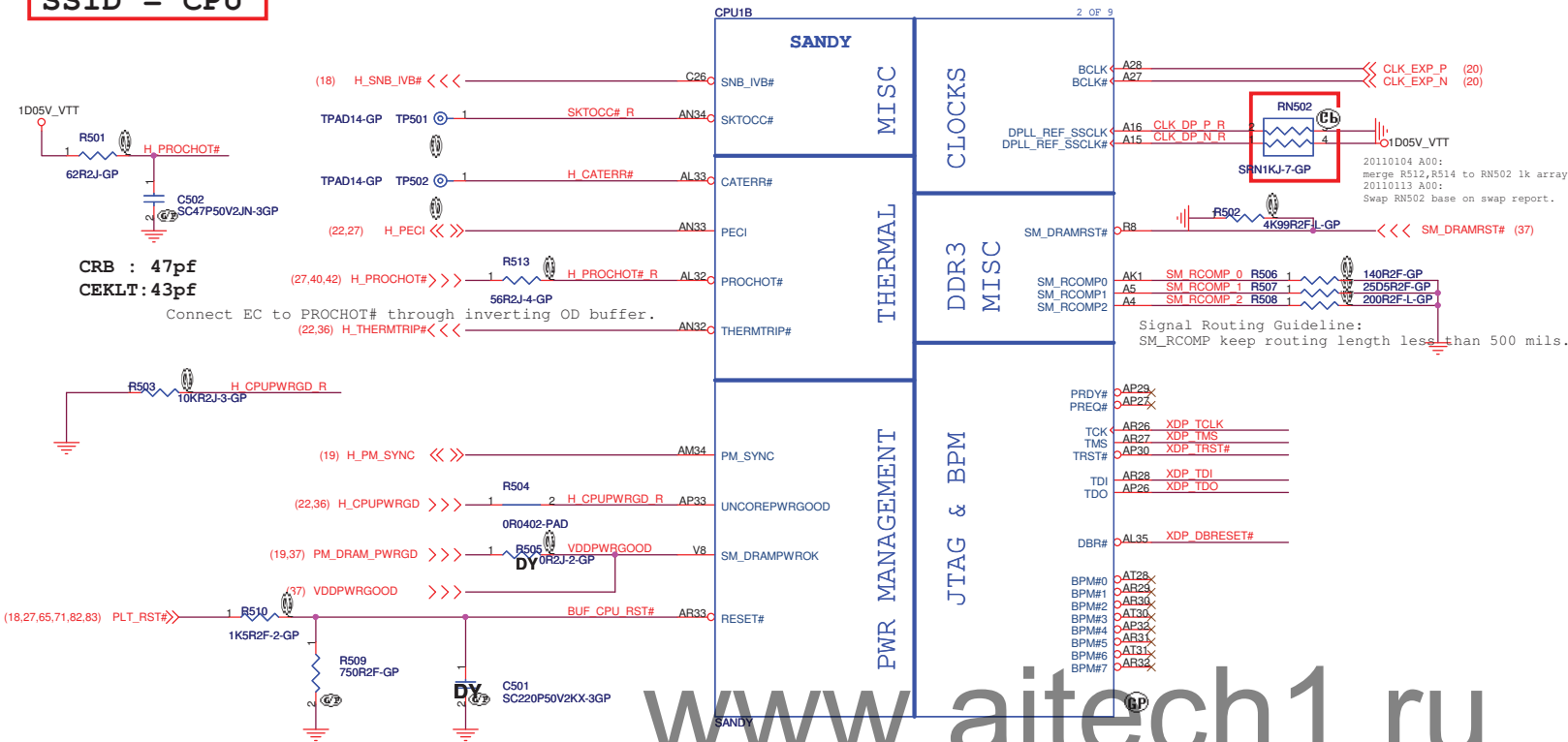
Stuff to disable internal graphics function for power saving.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

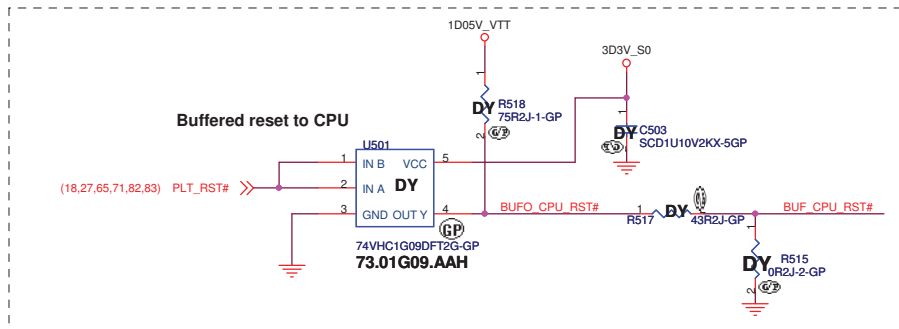
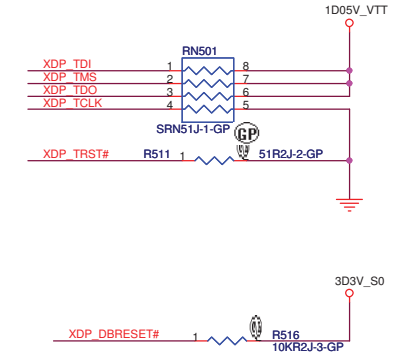
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



SSID = CPU



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor (power (~15 mW) may be wasted).

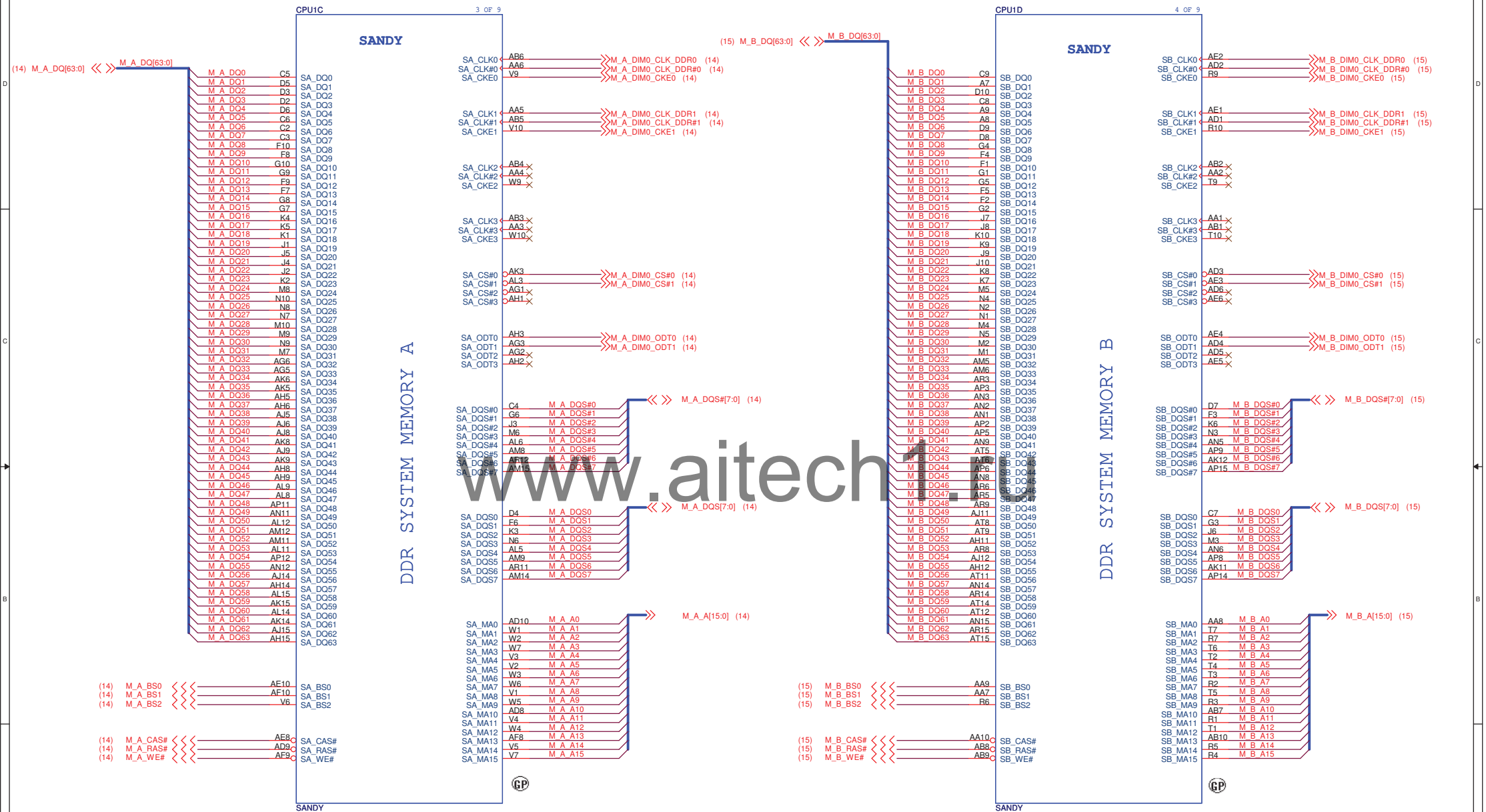


XDP_DBRESET# >>> XDP_DBRESET# (19)

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DELL		Wistron Corporation	
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Title			
CPU 2/7(THERMAL/CLOCK/PM)			
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SSID = CPU



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Title		CPU 3/7(DDR)	
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SSID = CPU

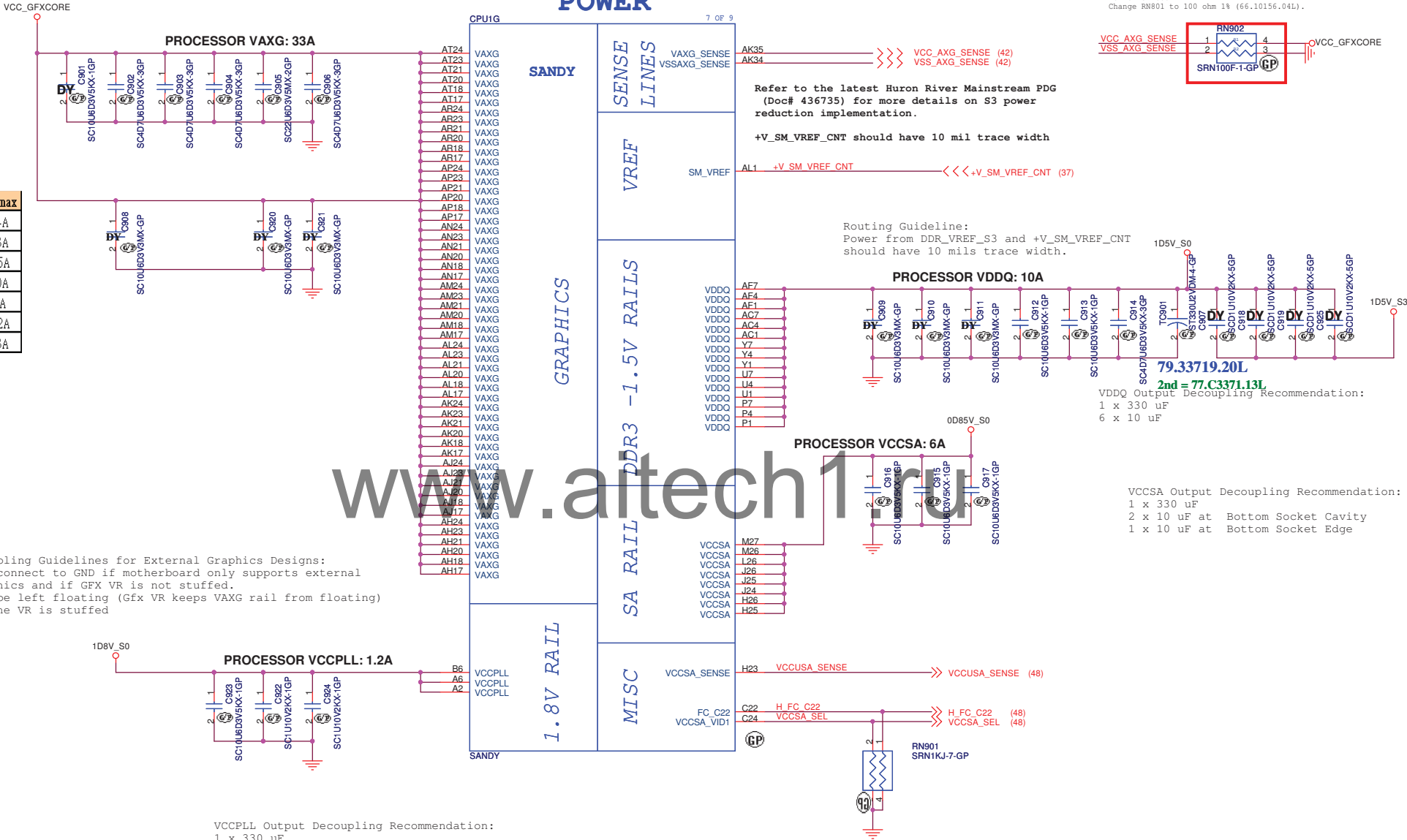
VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

Voltage Rail	Voltage	Iccmax
VCC_CORE(QQ)	0.8-1.35	94A
VCC_CORE(DC)	0.8-1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75-0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

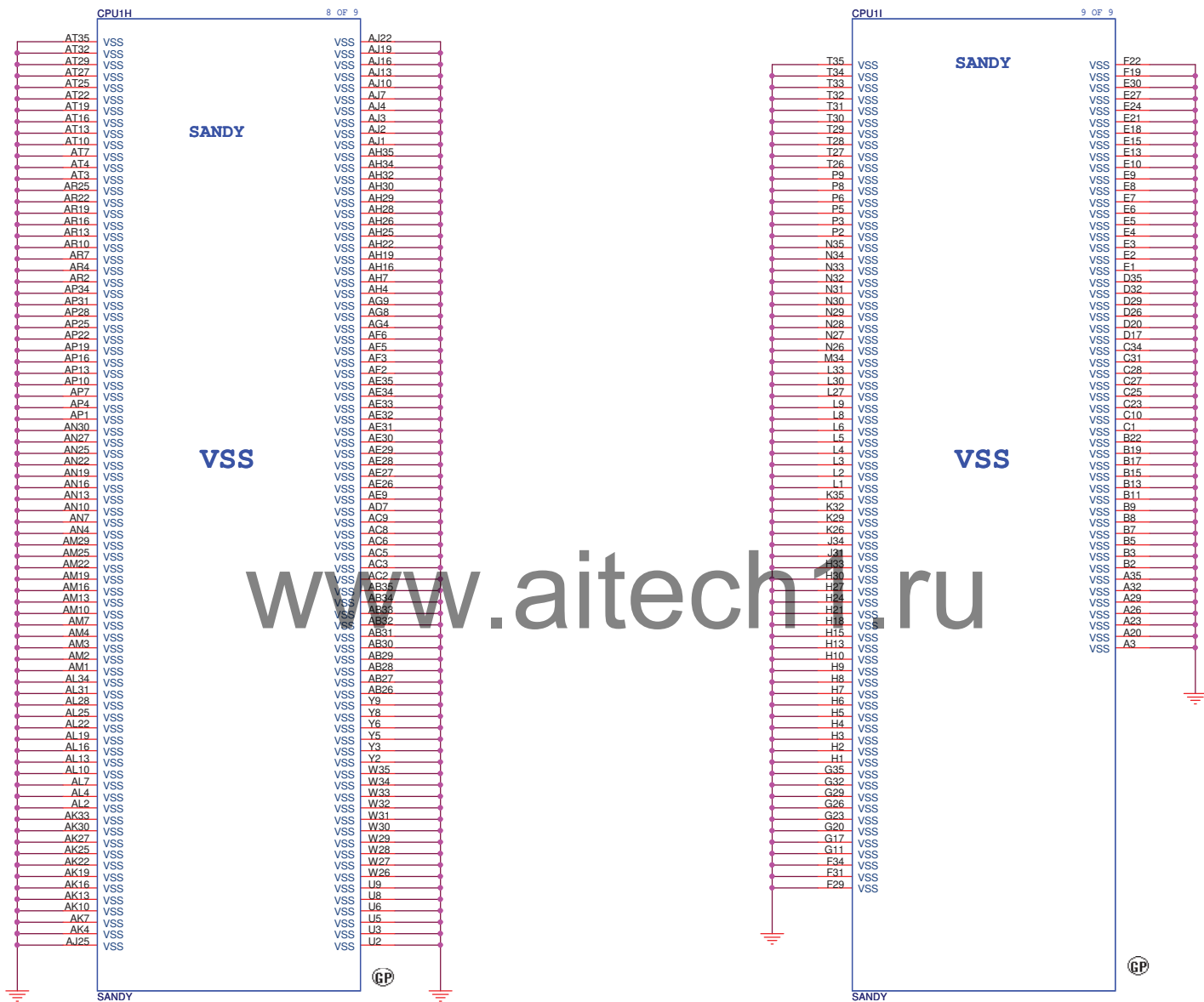
Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

POWER



SSID = CPU



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Remove the XDP connector for space saving 6/28

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XDP

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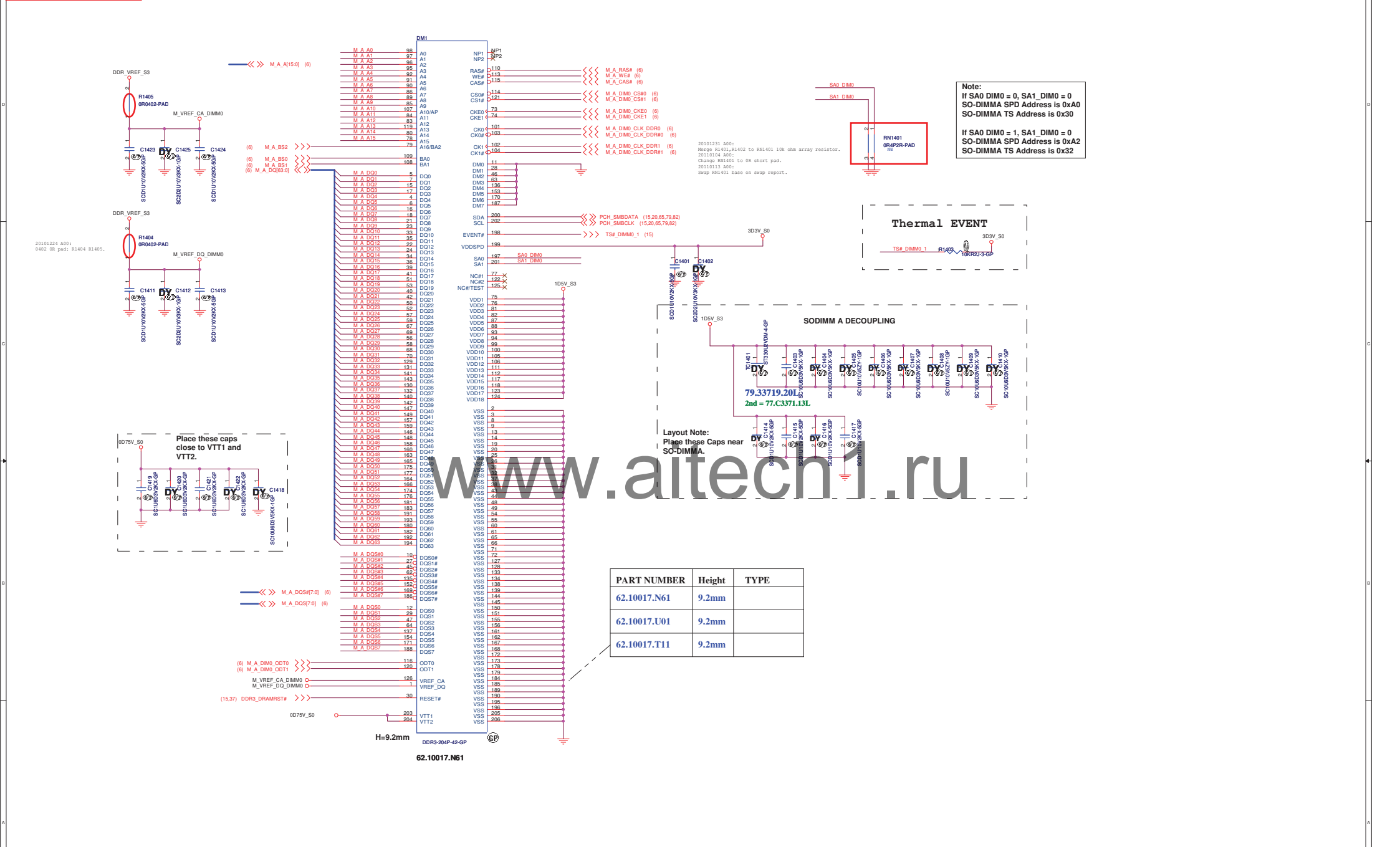
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Title

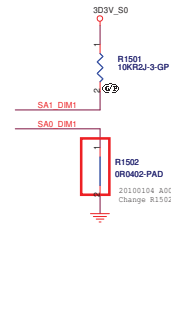
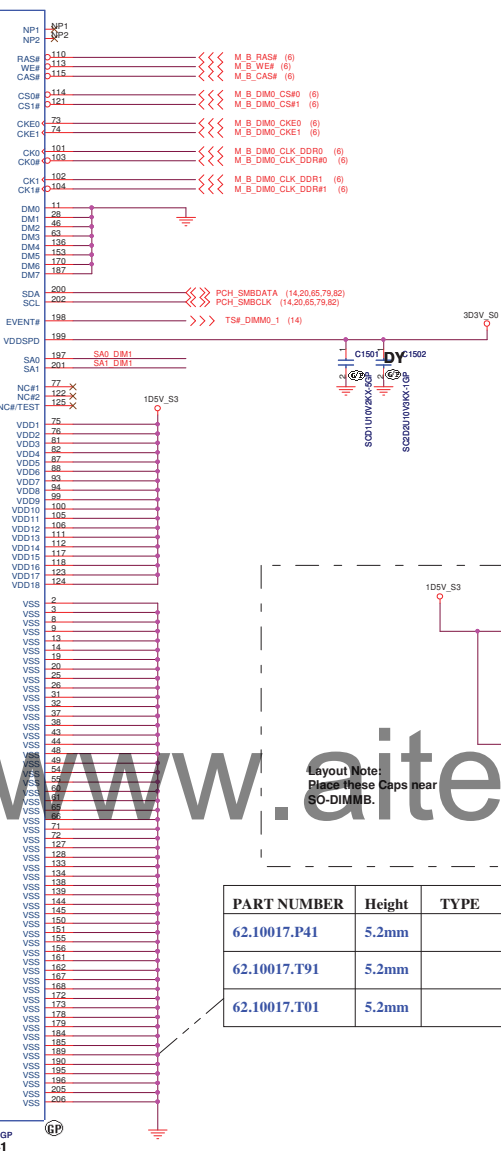
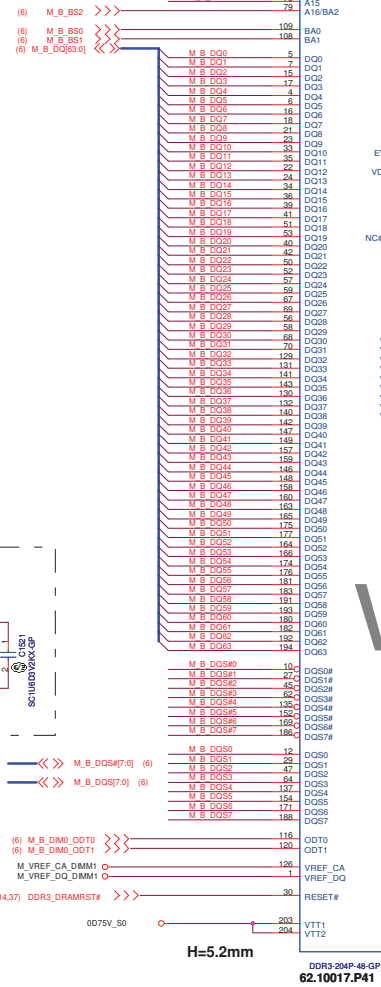
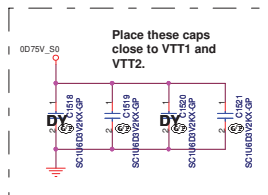
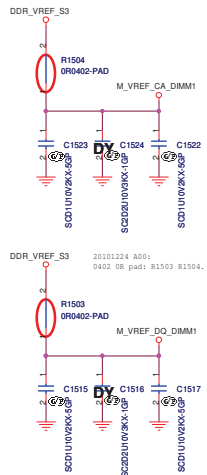
Reserved

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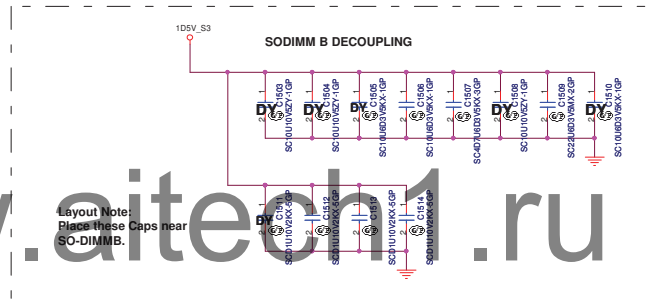


SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA




PART NUMBER	Height	TYPE
62.10017.P41	5.2mm	
62.10017.T91	5.2mm	
62.10017.T01	5.2mm	

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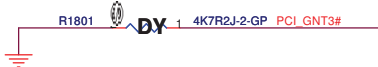
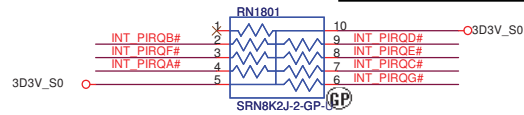
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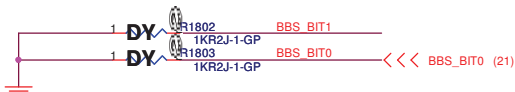
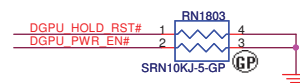
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USB 2.0 Overcurrent Pin Default Usage

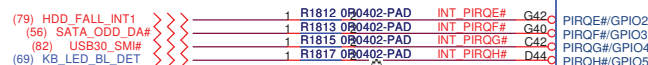
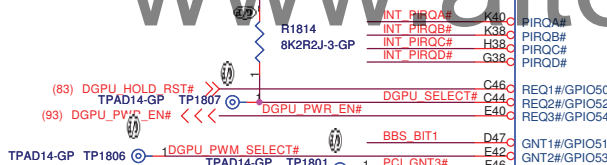
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used



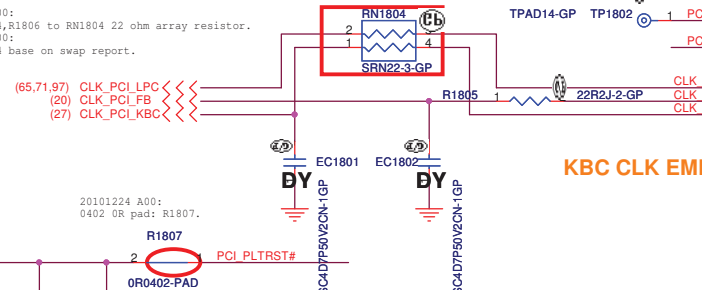
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



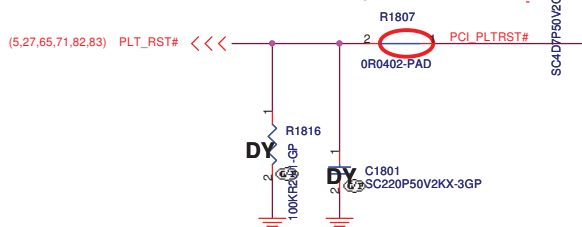
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



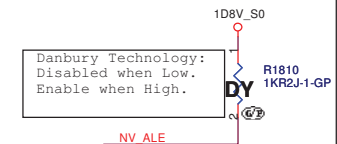
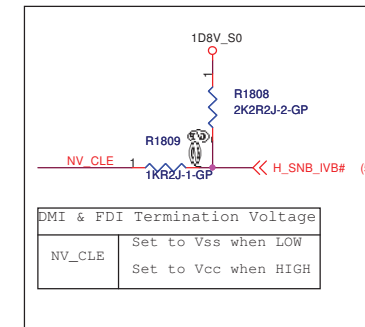
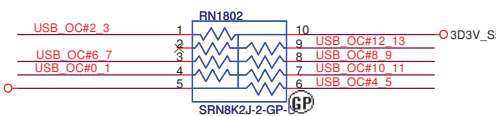
```
20101231 A00:
Merge R1804,R1806 to RN1804 22 ohm array resistor.
20110113 A00:
Swap RN1804 base on swap report.
```



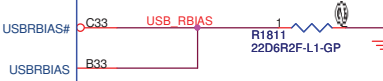
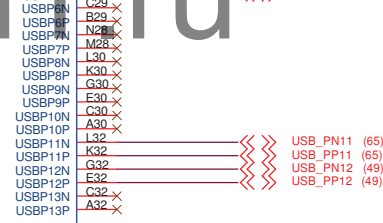
20101224 A00:
0402 0R pad: R1807.



OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)



✗ USB Ext. port 1 (HS)
✗ External debug port use on Huron river platform



USB Table

Pair	Device
0	X
1	E-SATA / USB Combo
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

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SSID = PCH

(4) DMI_RXN[3:0] <<<<
(4) DMI_RXP[3:0] <<<<
(4) DMI_TXN[3:0] <<<<
(4) DMI_TXP[3:0] <<<<

<<<< FDI_TXN[7:0] (4)
<<<< FDI_TXP[7:0] (4)

Deep S4/S5 Supported

Deep S4/S5 Not Supported

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.

(4) DMI_RXN0 <<<< BC24
(4) DMI_RXN1 <<<< BE20
(4) DMI_RXN2 <<<< BG18
(4) DMI_RXN3 <<<< BG20
(4) DMI_RXP0 <<<< BE24
(4) DMI_RXP1 <<<< BC20
(4) DMI_RXP2 <<<< BJ18
(4) DMI_RXP3 <<<< BJ20
(4) DMI_TXN0 <<<< AW24
(4) DMI_TXN1 <<<< AW20
(4) DMI_TXN2 <<<< BB18
(4) DMI_TXN3 <<<< AV18
(4) DMI_TXP0 <<<< AY24
(4) DMI_TXP1 <<<< AY20
(4) DMI_TXP2 <<<< AY18
(4) DMI_TXP3 <<<< AU18

PCH1C

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Cougar
Point

DMI

FDI

FDI_RXN0 BJ14 <<<< FDI_TXN0 (4)
FDI_RXN1 AY14 <<<< FDI_TXN1 (4)
FDI_RXN2 BE14 <<<< FDI_TXN2 (4)
FDI_RXN3 BH13 <<<< FDI_TXN3 (4)
FDI_RXN4 BJ12 <<<< FDI_TXN4 (4)
FDI_RXN5 BG10 <<<< FDI_TXN5 (4)
FDI_RXN6 BG9 <<<< FDI_TXN6 (4)
FDI_RXN7 BG14 <<<< FDI_TXP0 (4)
FDI_RXP1 BB14 <<<< FDI_TXP1 (4)
FDI_RXP2 BE14 <<<< FDI_TXP2 (4)
FDI_RXP3 BG13 <<<< FDI_TXP3 (4)
FDI_RXP4 BE12 <<<< FDI_TXP4 (4)
FDI_RXP5 BG12 <<<< FDI_TXP5 (4)
FDI_RXP6 BJ10 <<<< FDI_TXP6 (4)
FDI_RXP7 BH9 <<<< FDI_TXP7 (4)

FDI_INT AW16 <<<< FDI_INT (4)
FDI_FSYNCO AV12 <<<< FDI_FSYNCO (4)
FDI_FSYNCO BC10 <<<< FDI_FSYNCO (4)
FDI_LSYNCO AV14 <<<< FDI_LSYNCO (4)
FDI_LSYNCO BB10 <<<< FDI_LSYNCO (4)

VccDSW3_3

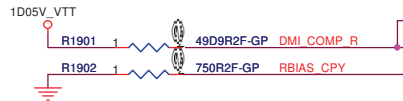
DPWROK

VccSUS3_3

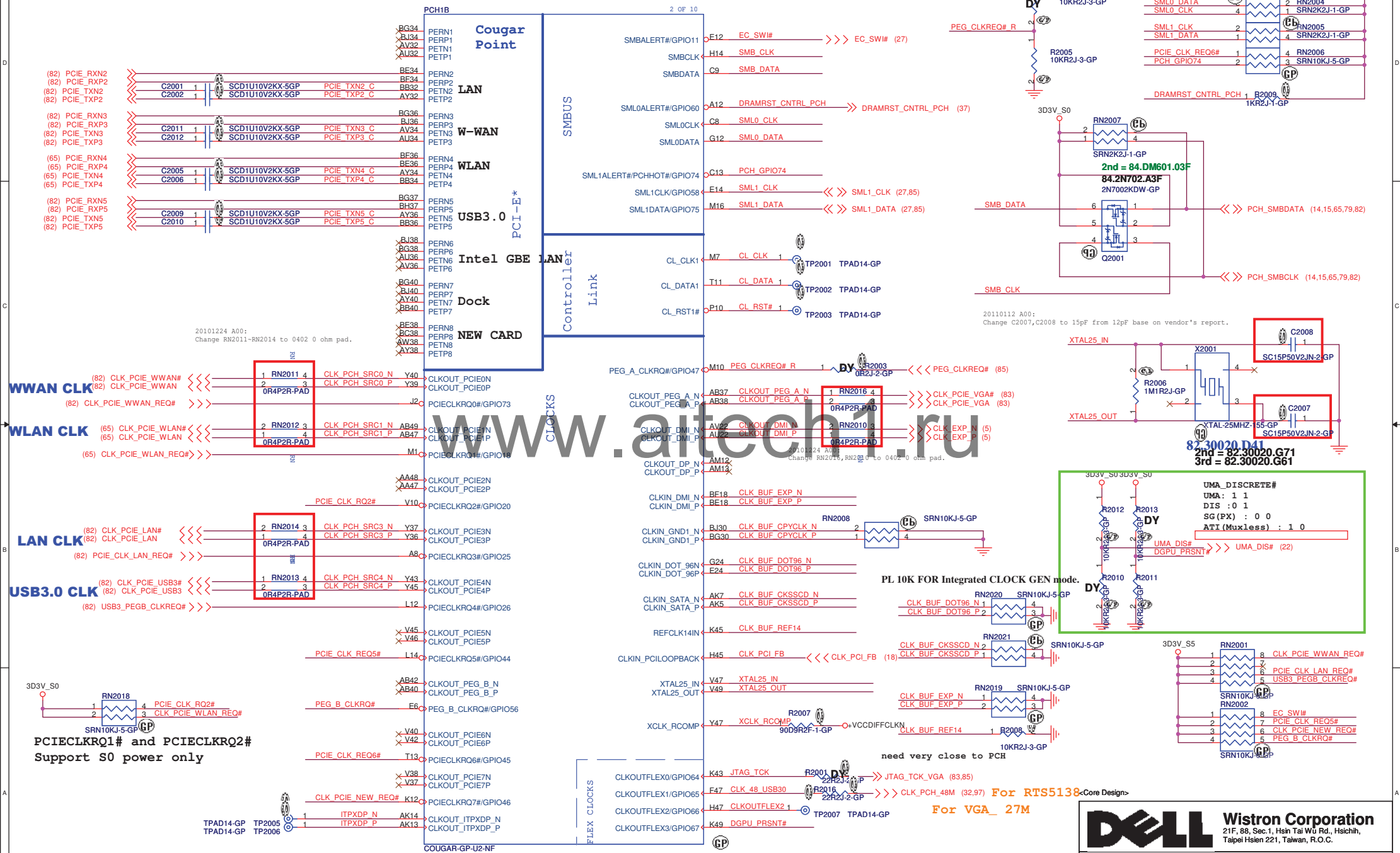
RSMRST#

For platforms not supporting Deep S4/S5

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30

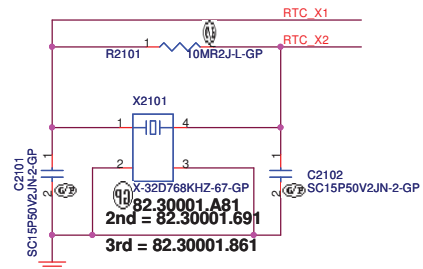


SSID = PCH

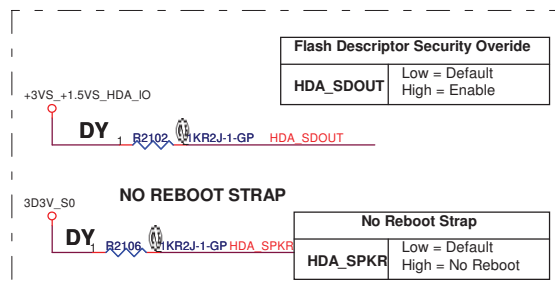
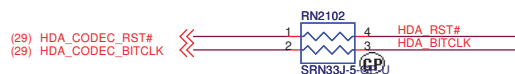


- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

SSID = PCH

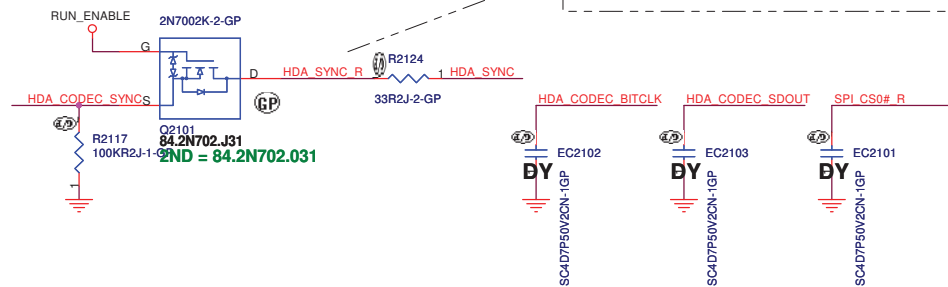


(29) HDA_CODEC_SYNC 33R2J-2-GP R2122 HDA_SYNC
(29) HDA_CODEC_SDOUT 33R2J-2-GP R2123 HDA_SDOUT



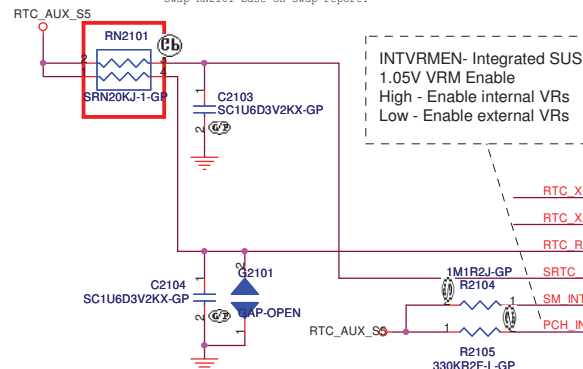
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled high for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

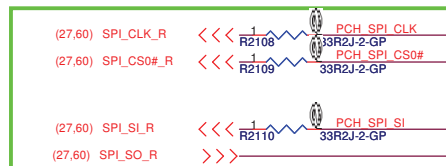
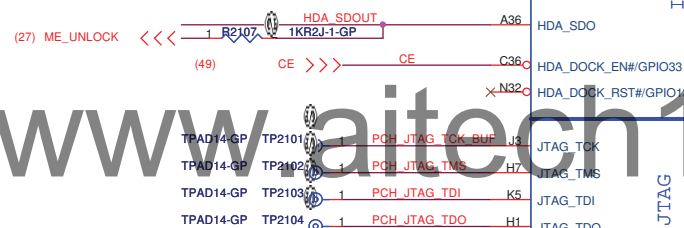


```
20110110 A00:
Merge R2115,R2116 to RN2101.
20110113 A00:
Swap RN2101 base on swap report.
```

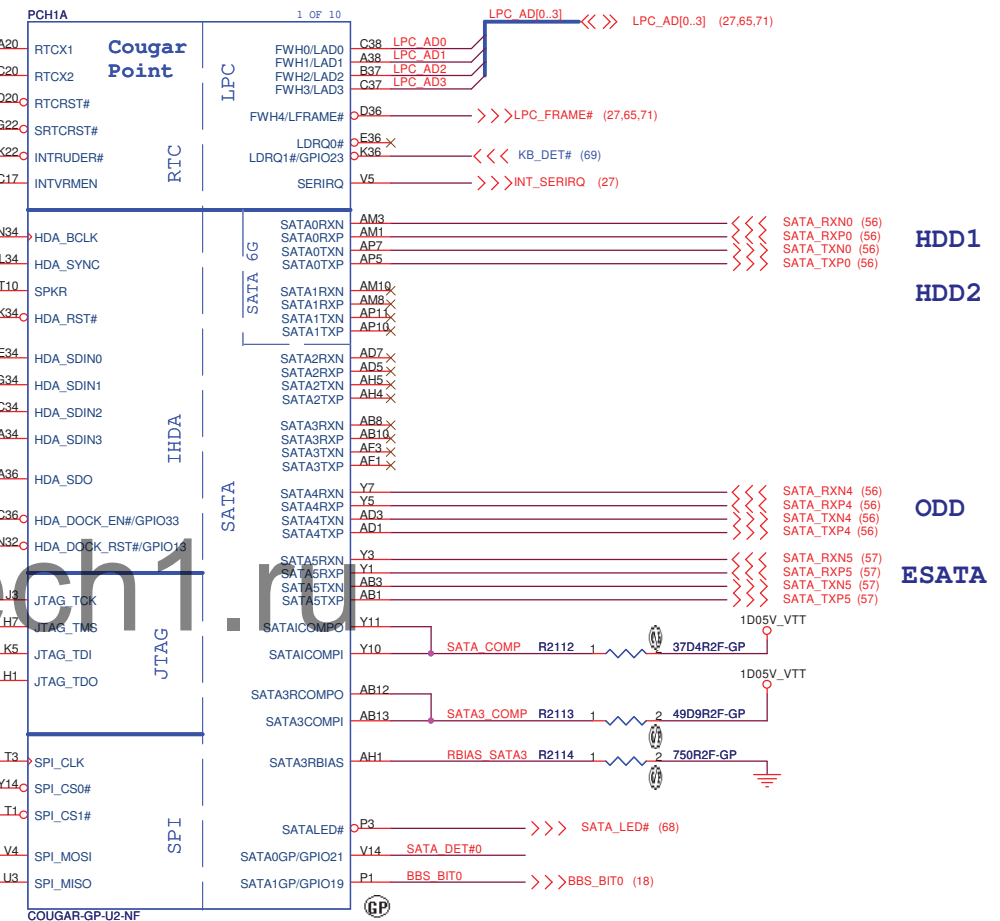
INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs



Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



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Title **PCH 5/9(SPI/BTC/LPC/SATA/IHDA)**

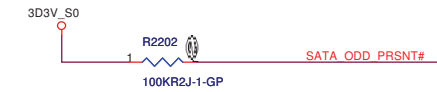
Size	Document Number	Rev
	Nirvana 13	A00

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SSID = PCH

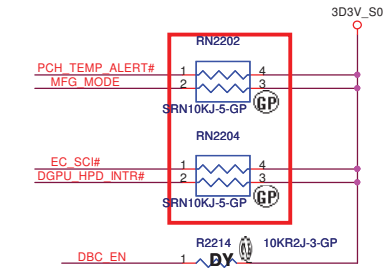
Note:
For PCH debug with XDP, need to NO STUFF R2218

	GSENSOR_ADI	GSENSOR_ST
R2205	DY	10K
R2206	100K	DY

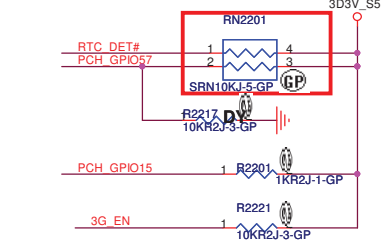


GPI027 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

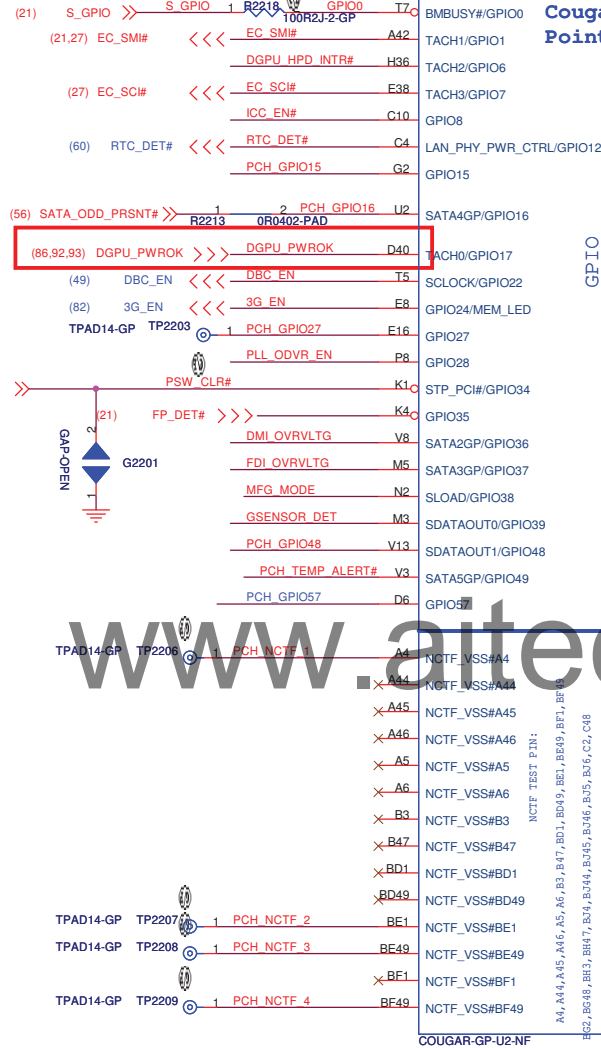
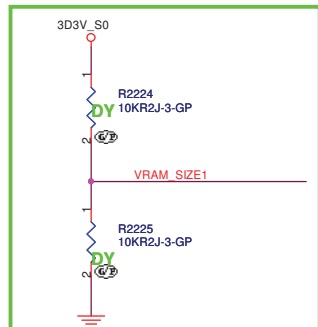
20100104 A00:
Merge RN2201,R2222,R2223 to 10k array resistor.
20110113 A00:
Combine PCH_TEMP_ALERT#,MFG_MODE to RN2202.
Combine EC_SCI#,DGPU_HPD_INTR# to RN2204



20100104 A00:
Merge RN2215,R2216 to RN2201 10k array resistor.



For thermal sensor detection.



PLL ON DIE VR ENABLE

NOTE:This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN DY 1 R2212 10KR2J-1-GP

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4
should not float on the motherboard. They should
be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE

GPI037 (FDI_OVRVLTG) LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE

GPI036 (DMI_OVRVLTG) LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable

ICC_EN# HIGH (R2211 DY)- DISABLED [DEFAULT]

LOW (R2211)- ENABLED

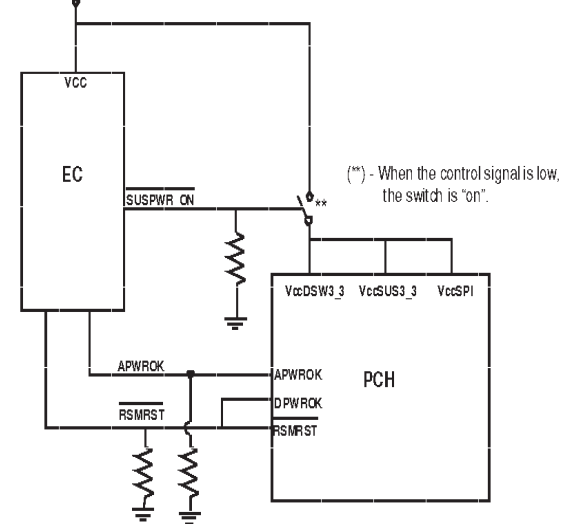
GPI08 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

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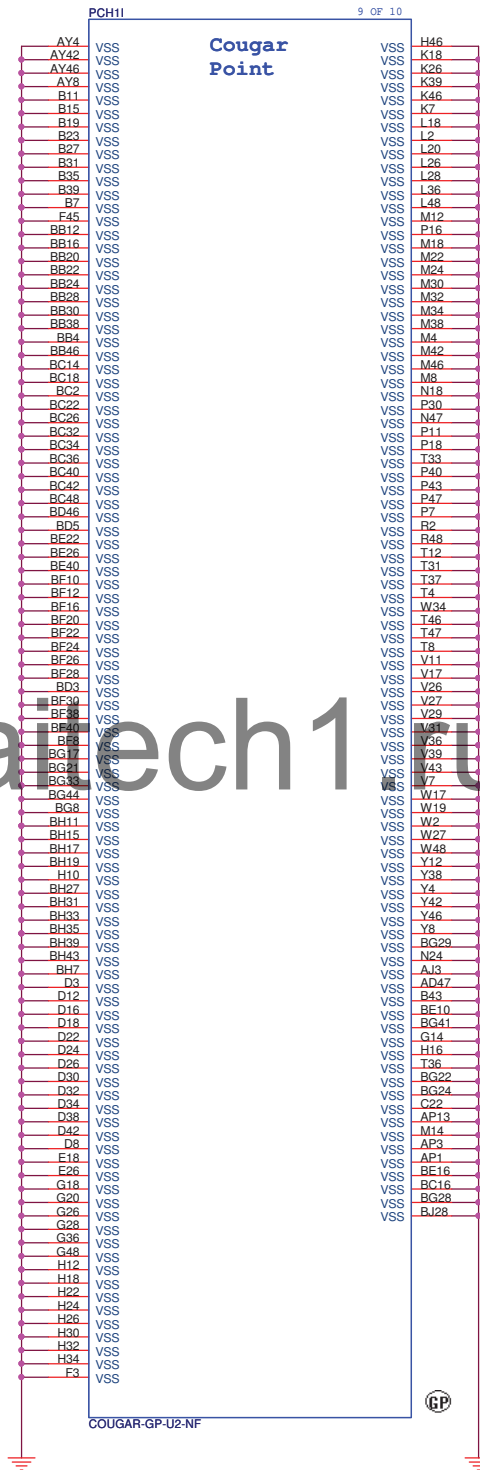
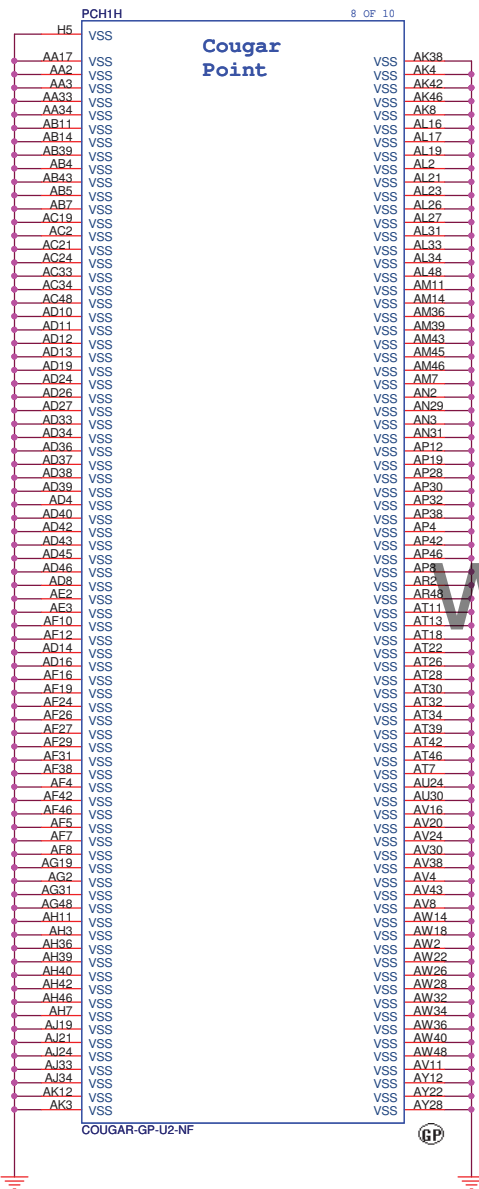
Title **PCH 6/9(GPIO/CPU)**
Size Document Number **Nirvana 13** Rev **A00**
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6A



<div>  <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div>			
Title			
<div> <div>PCH 7/9(POWER1)</div> <div>Nirvana 13</div> </div>			
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SSID = PCH



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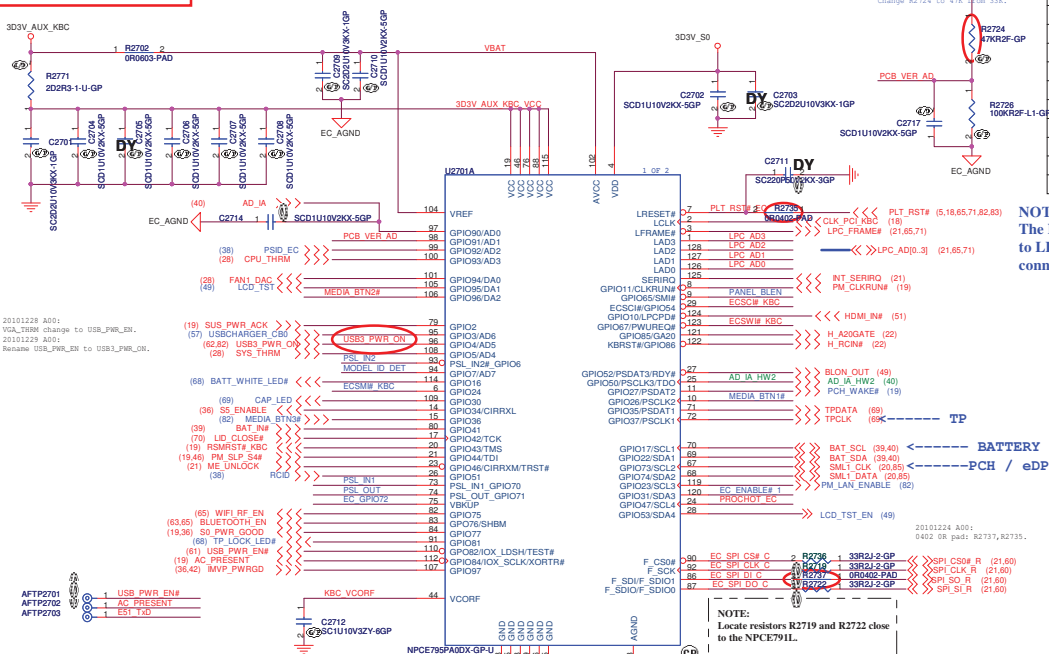
Title

Reserved

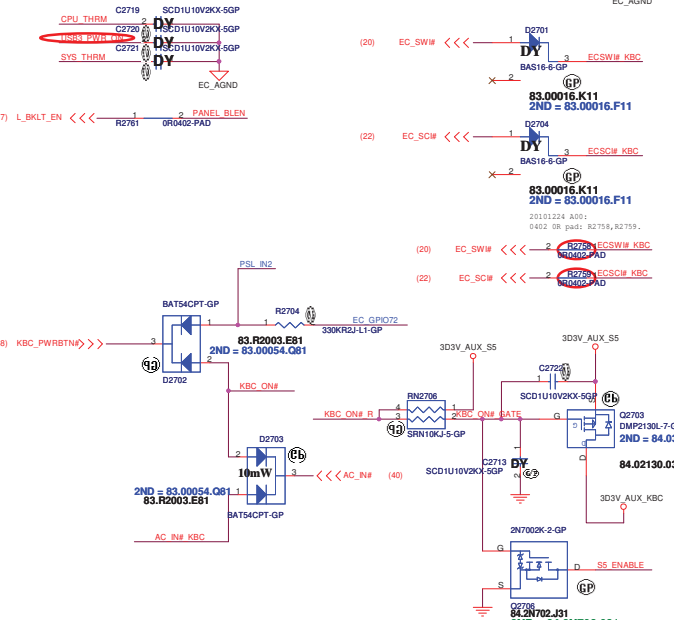
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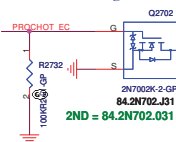
SSID = KBC



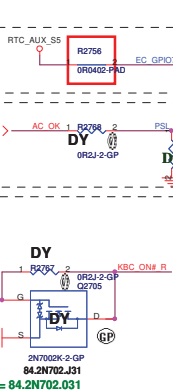
ROSA Multi GPIO setting



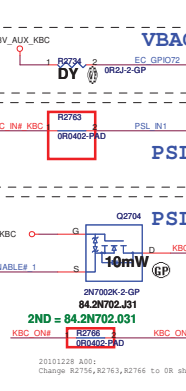
EC_GPIO47 High Active



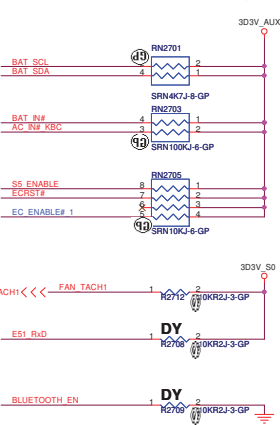
PSL SOLUTION



10mW SOLUTION

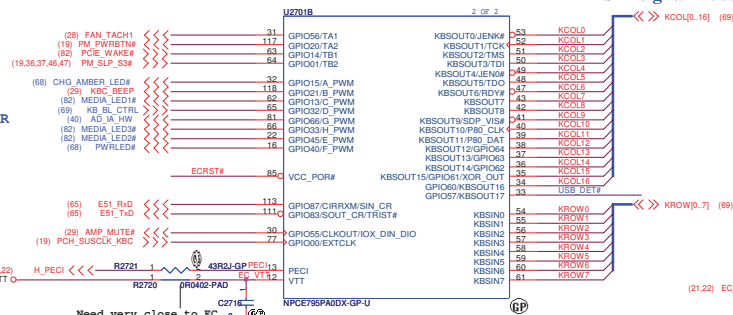


EC GPIO standard PH/PL



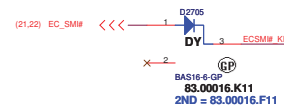
PCB Version A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

NOTES:
The NPCE795P GPIO/PWM outputs that are connected to LEDs have high drive buffers (20mA) and can be connected directly to the LEDs.



NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

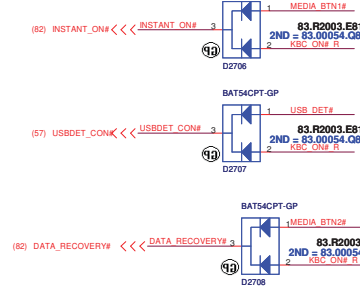
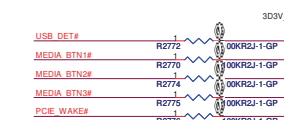
NOTE:
Connect GND and AGND planes via either
a 0-ohm resistor or one point layout connection.



20101224 A00:
0402 OR pad: R2760.



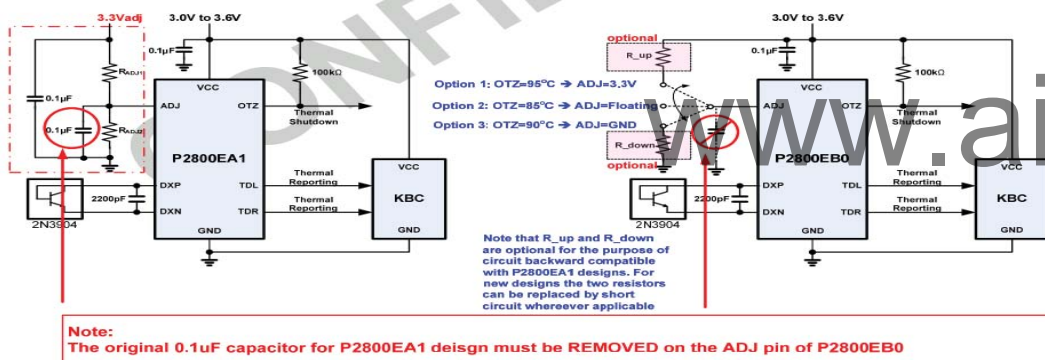
MEDIA BUTTON CONTROL



NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#AC_PRESENT,E51_TXD.

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

Thermal sensor P2800



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 $\pm 1\%$ Series)

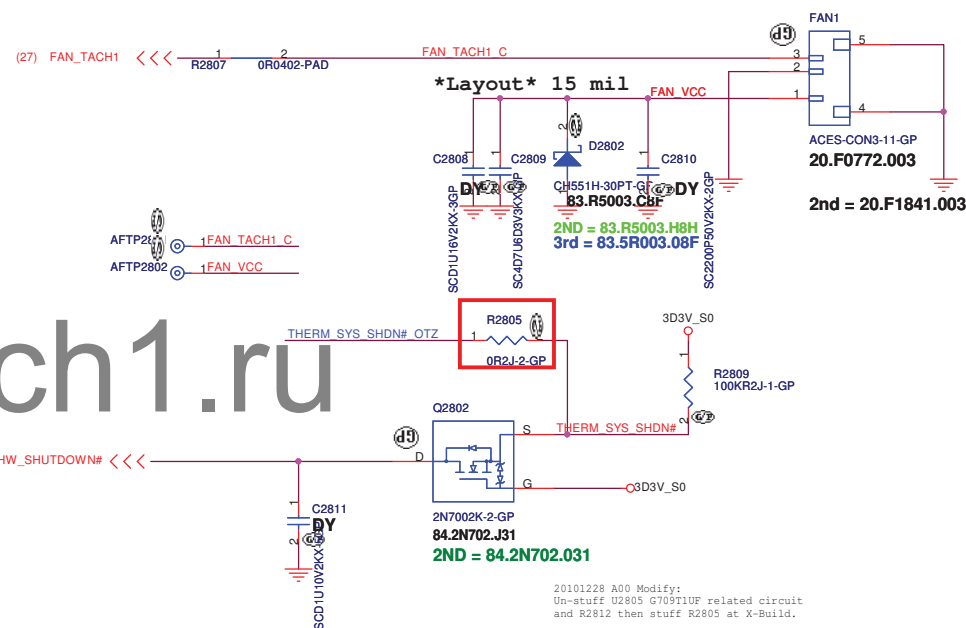
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

FUNCTION

h (P2793A).
 functioning when /FON voltage is above 1.6V.
 low(<0.4V), VOUT will be fully on

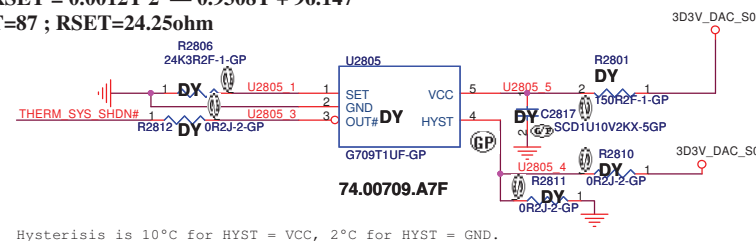
this input pin controls the VOUT voltage by

PIN#	I/O	FUNCTION
1	I	Internal Pull-high (P2793A). The IC will be functioning when /FON voltage is above 1.6V When /FON is low(<0.4V), VOUT will be fully on
2	O	Input Voltage
3	O	Output Voltage
4	I	The voltage on this input pin controls the VOUT voltage by the formula: $VOUT = 1.6 * VSET$ When VSET is under 0.8V the IC will be shutdown
5,6,7,8	O	Ground



$$\text{RSET} = 0.0012T^2 - 0.9308T + 96.147$$

T=87 ; RSET=24.25ohm



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Title

THERMAL P2800 / Fan control

Size

Document Number

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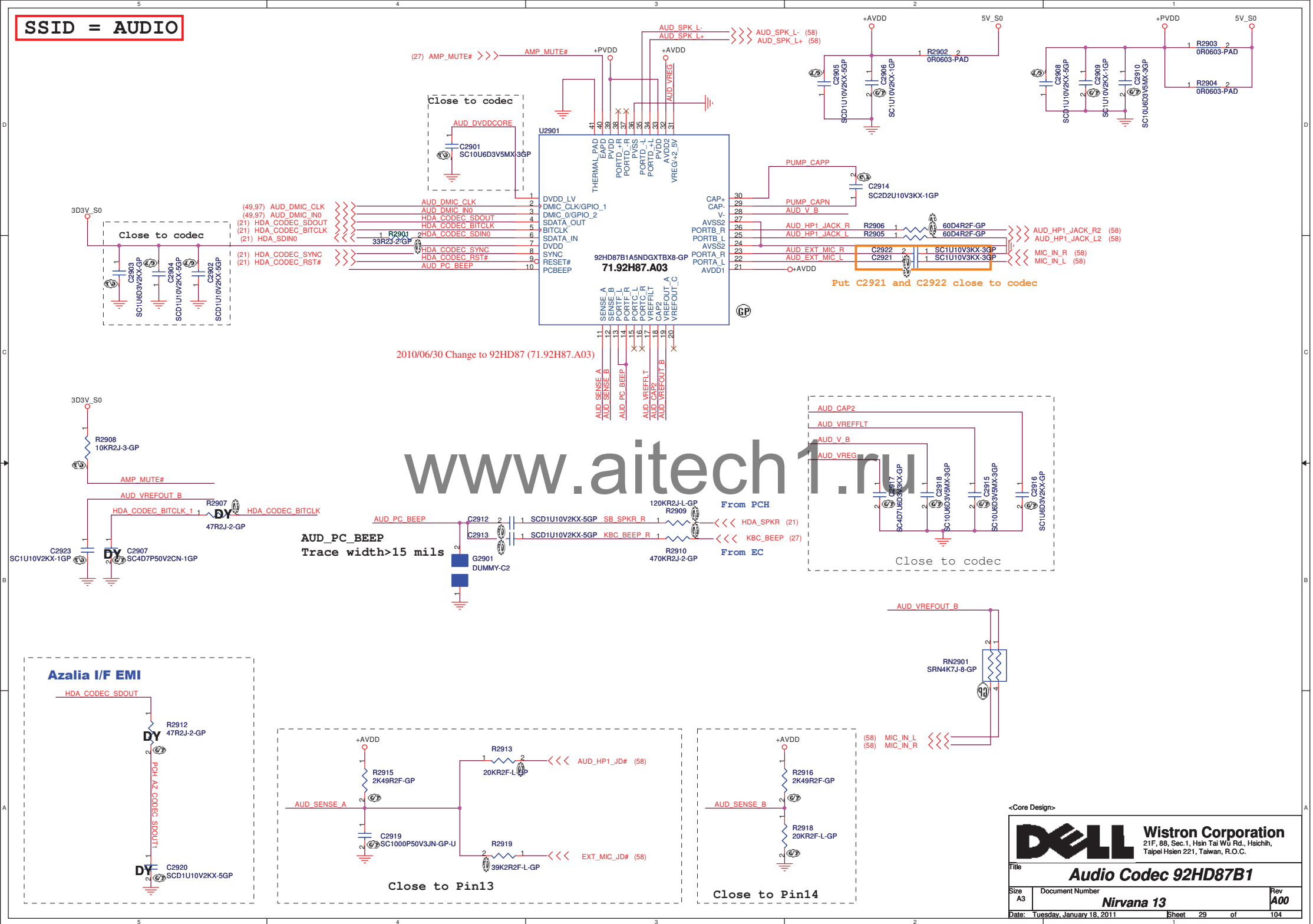
Rev

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SSID = AUDIO



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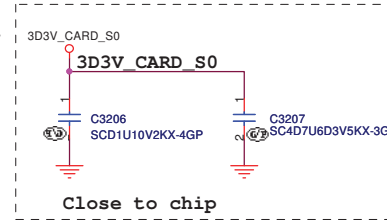
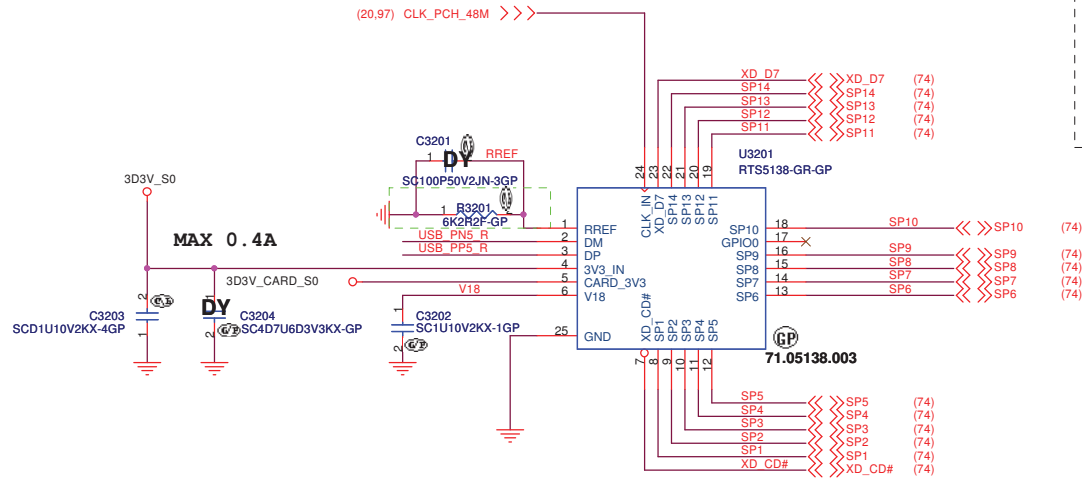
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SSID = SDIO

48MHz clock input trace of characteristic impedance (Z_0) must be $50 \pm 15\%$.



PIN	TYPE	FUNCTION	RTS5138 NET
1	SD	SD-DAT2	SP13
2	SD	SD-CD/DAT3	SP12
3	MMC_PLUS	MMC-DAT4	SP11
4	SD	SD-CMD	SP10
5	MMC_PLUS	MMC-DAT5	SP9
6	SD	SD-VSS	POWER
7	SD	SD-VDD	POWER
8	MemoryStick	MS-VSS	POWER
9	MemoryStick	MS-VCC	POWER
10	MemoryStick	MS-SCLK	SP1
11	MemoryStick	MS-DAT3	SP5
12	MemoryStick	MS-INS	SP2
13	MemoryStick	MS-DAT2	SP8
14	MemoryStick	MS-DAT0	SP9
15	MemoryStick	MS-DAT1	SP12
16	MemoryStick	MS-BS	SP14
17	MemoryStick	MS-VSS	POWER
18	SD	SD-CLK	SP8
19	MMC_PLUS	MMC-DAT6	SP7
20	SD	SD-VSS	POWER
21	MMC_PLUS	MMC-DAT7	SP5
22	SD	SD-DAT0	SP4
23	SD	SD-DAT1	SP3
24	SD	SD-COM(SW)	
25	SD	SD-CD(SW)	SP6
26	XD	XD-GND	POWER
27	XD	XD-CD	XD_CD#
28	XD	XD-R/B	SP1
29	XD	XD-RE	SP2
30	XD	XD-CE	SP3
31	XD	XD-CLE	SP4
32	XD	XD-ALE	SP5
33	XD	XD-WE	SP6
34	XD	XD-WF	SP7
35	XD	XD-GND	POWER
36	XD	XD-D0	SP8
37	XD	XD-D1	SP9
38	XD	XD-D2	SP10
39	XD	XD-D3	SP11
40	XD	XD-D4	SP12
41	XD	XD-D5	SP13
42	XD	XD-D6	SP14
43	XD	XD-D7	XD-D7
44	XD	XD-VCC	POWER
45	SD	SD-WF(SW)	SP1

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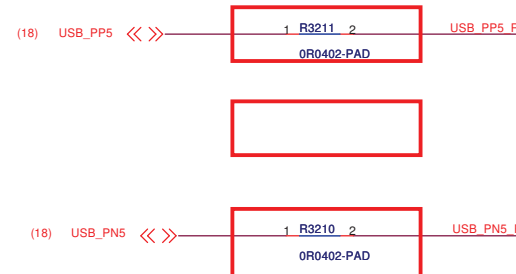
The maximum range of the PMOS output current

1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

POWER TRACE

1. RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2. RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3. RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum). Keep the trace routing lengths as short as possible.
4. RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5. RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6. De-coupling and Bulk capacitor should place near to RTS5138 chip and Combo Socket.
7. It is recommended that use of ferrites bead on power trace.
8. Via size: Pad \geq 32 mils, Finished hole \geq 16 mils.

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Z_{diff}) is $90\Omega \pm 10\%$



20101227 A00:
Change R3210, R3211 to 0R 0402 pad.
20100104 A00:
Remove TR3201.

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Title **Card Reader RTS5138**


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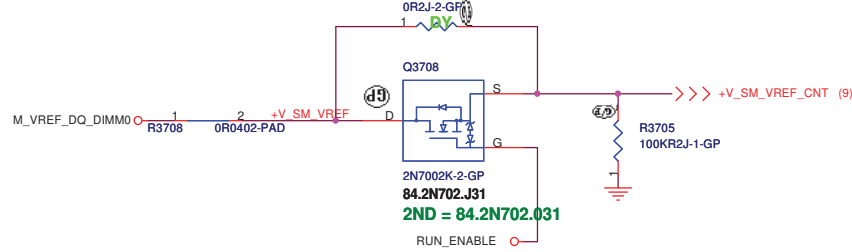
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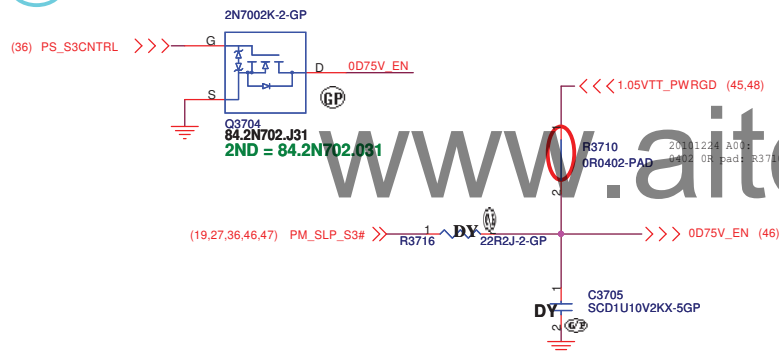
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Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



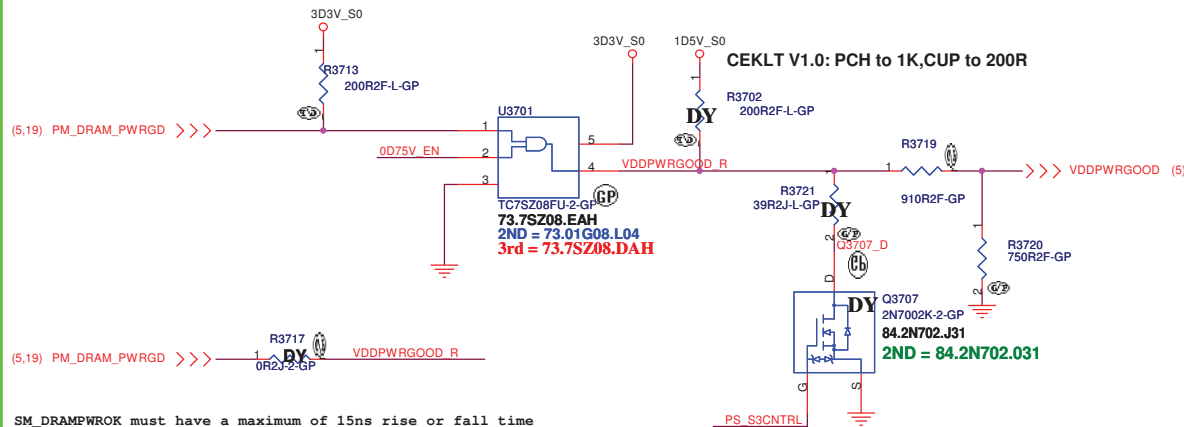
5 S3 Power Reduction



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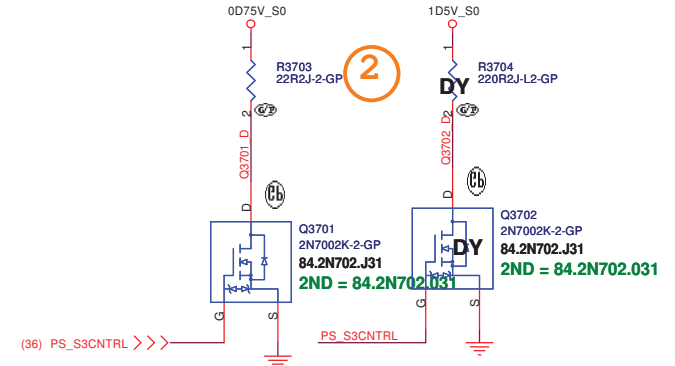
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

CEKLT V1.0: PCH to 1K,CUP to 200R

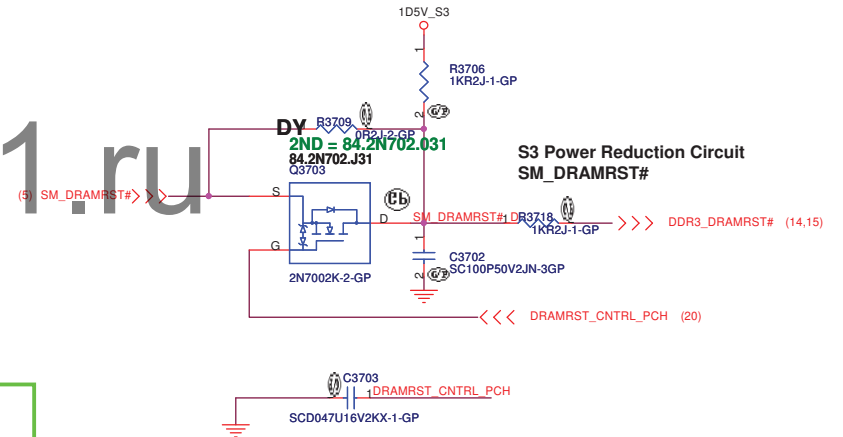


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



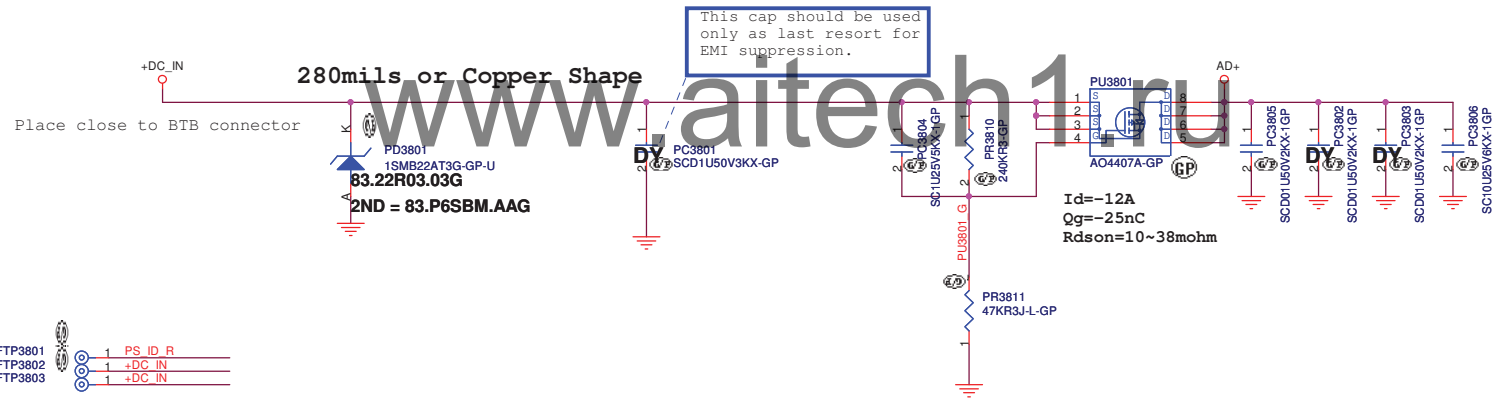
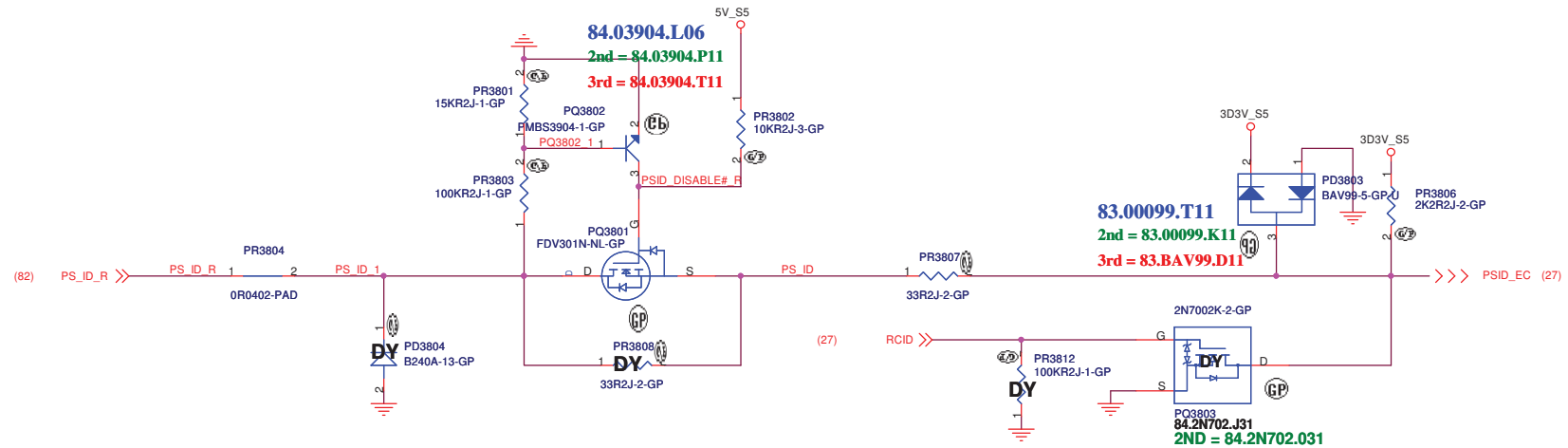
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



<Core Design>

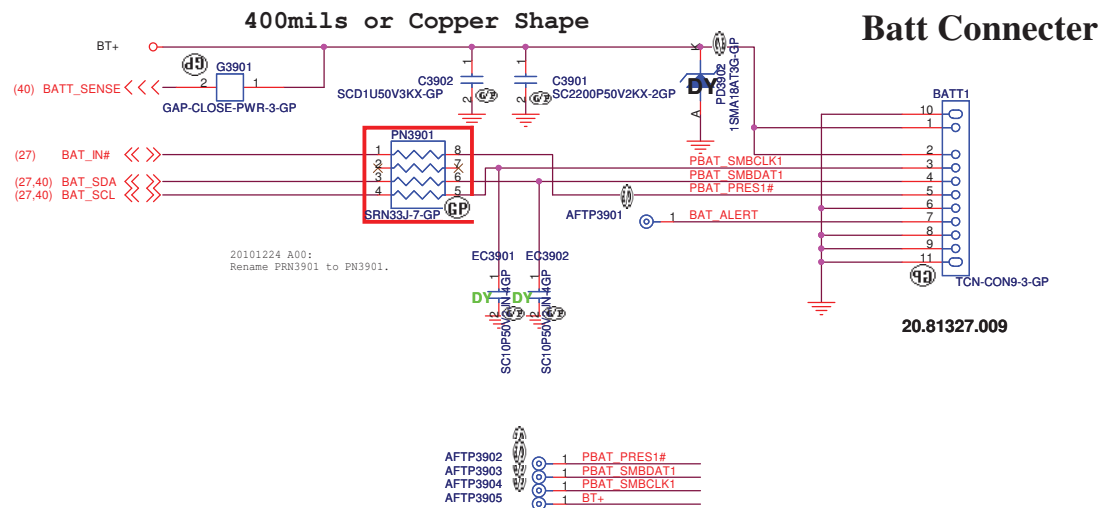
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Title		
S3 Power Reduction		
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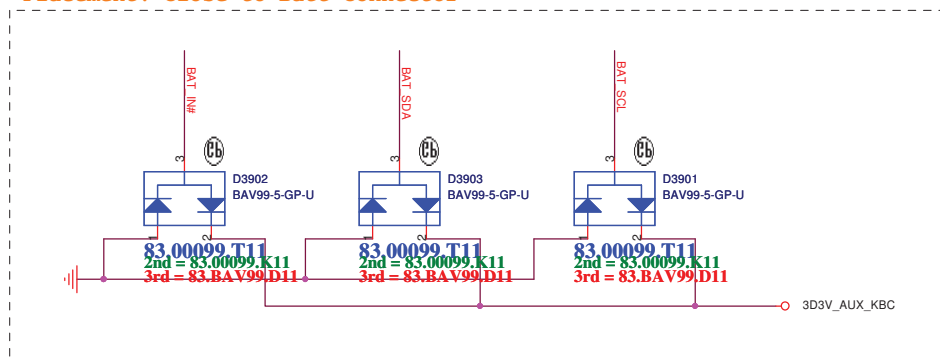
AFTP3801 PS_ID_R
AFTP3802 +DC_IN
AFTP3803 +DC_IN

<Core Design>



For actual location, need to be swap all pin

Placement: Close to Batt Connector



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Title

BATT CONN

Size
A3

Document Number

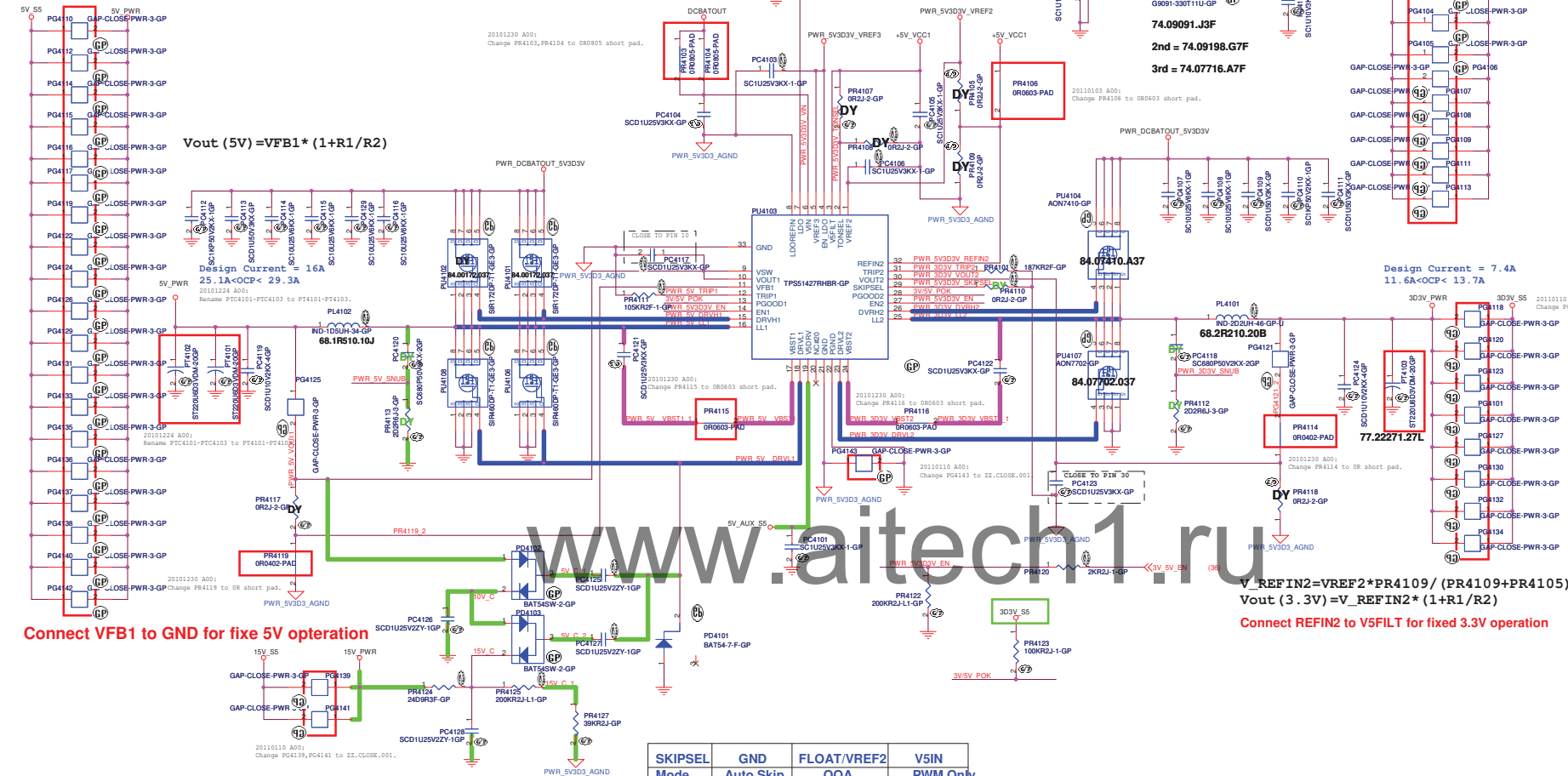
Nirvana 13

Rev
A00

Date: Tuesday, January 18, 2011

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20101010 A001
Change PG4110,PG4112,PG4114-PG4119,PG4122,PG4126,PG4129,PG4131,PG4133,PG4135-PG4138,PG4140,PG4142 to Z2.CLOSE.001.



$$V_{out} (5V) = V_{FB1} * (1 + R1/R2)$$

Design Current = 16A
25.1A < OCP < 29.3A

Design Current = 7.4A
11.6A < OCP < 13.7A

Connect VFB1 to GND for fixe 5V operation

$$V_{REFIN2} = V_{REF2} * PR4109 / (PR4109 + PR4105)$$

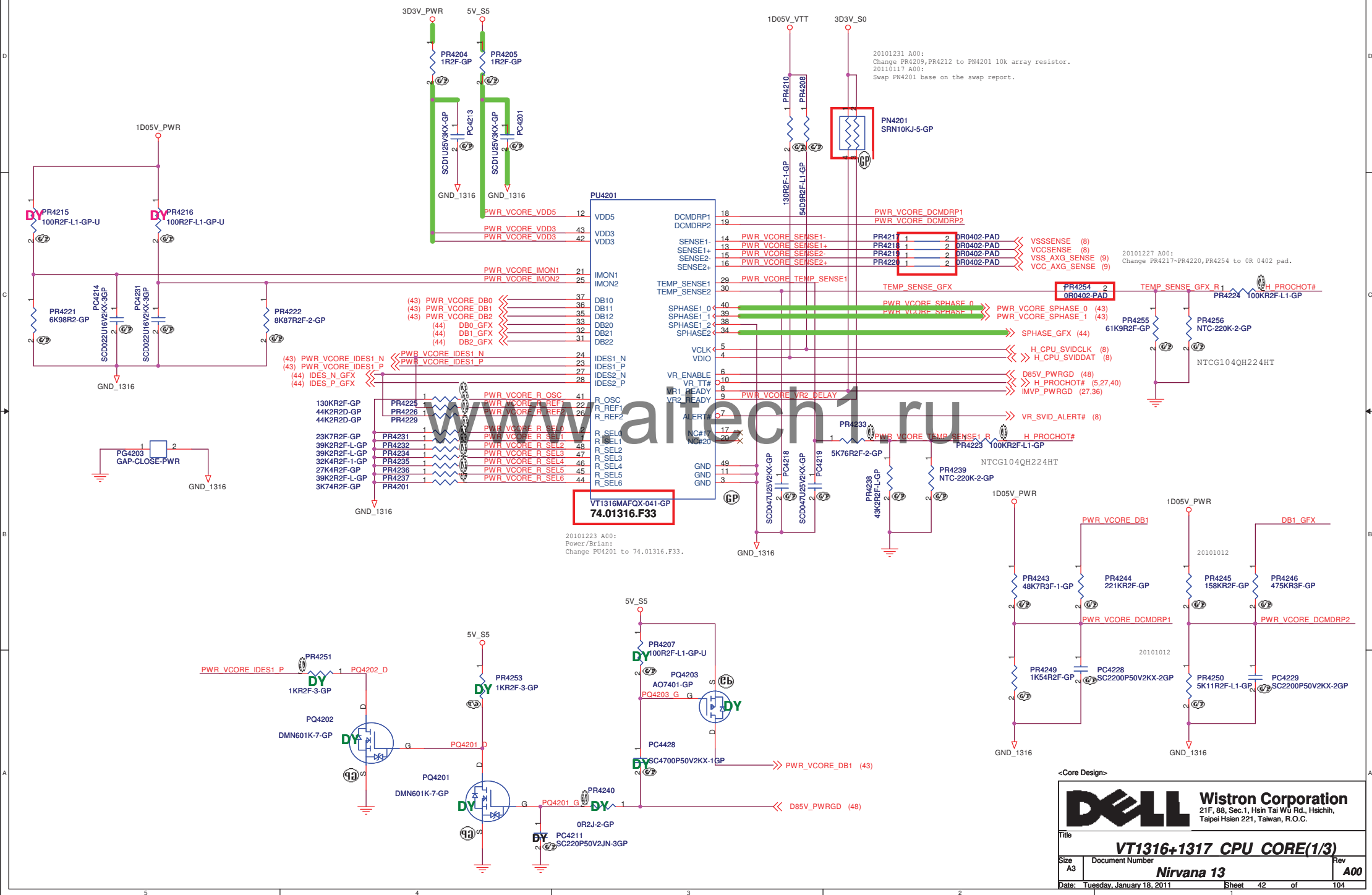
$$V_{out} (3.3V) = V_{REFIN2} * (1 + R1/R2)$$

Connect REFIN2 to V5FILT for fixed 3.3V operation

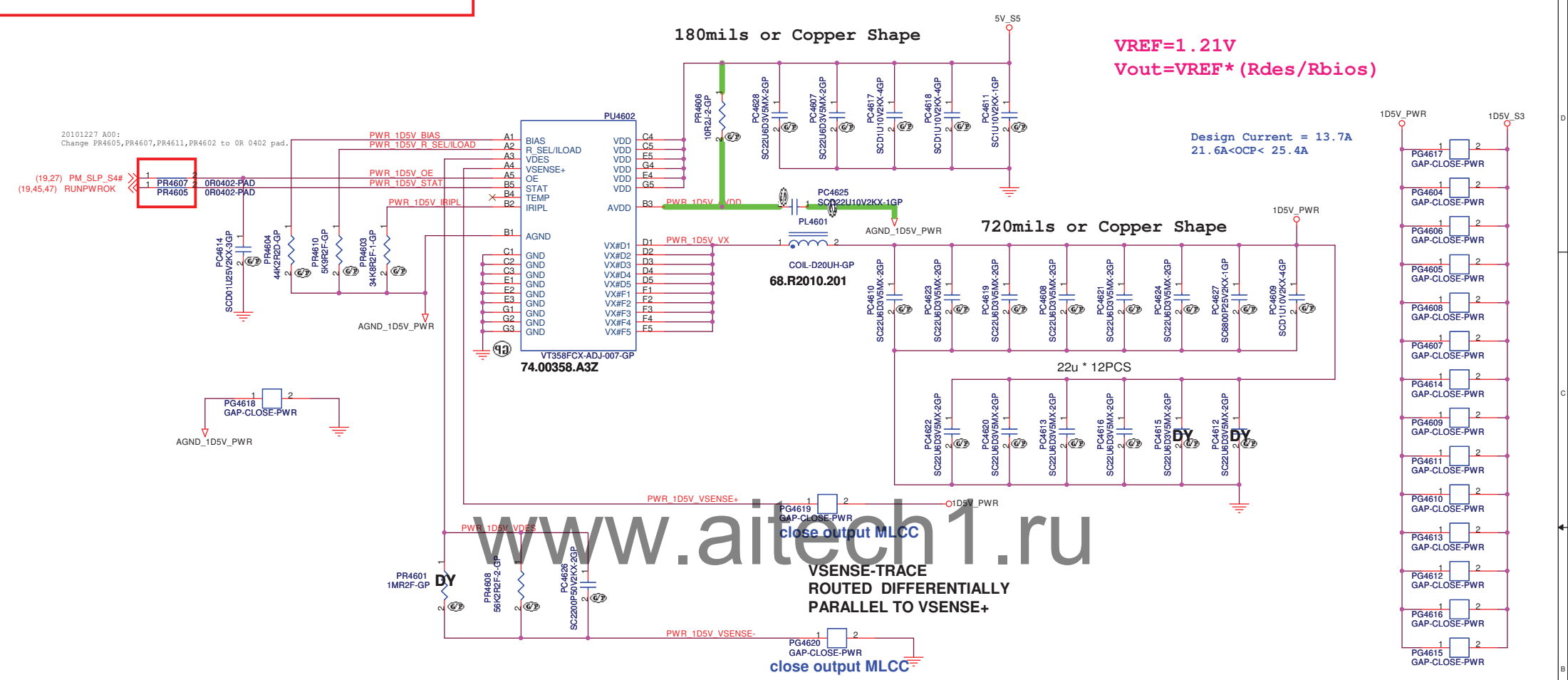
SKIPSEL Mode	GND Auto Skip	FLOAT/VREF2 OOA.	V5IN PWM Only
Ch1	400 kHz	400 kHz	200 kHz
Ch2	500 kHz	300 kHz	300 kHz

- 1A= 40mils
- 0.5A= 20mils
- 0.375A= 15mils

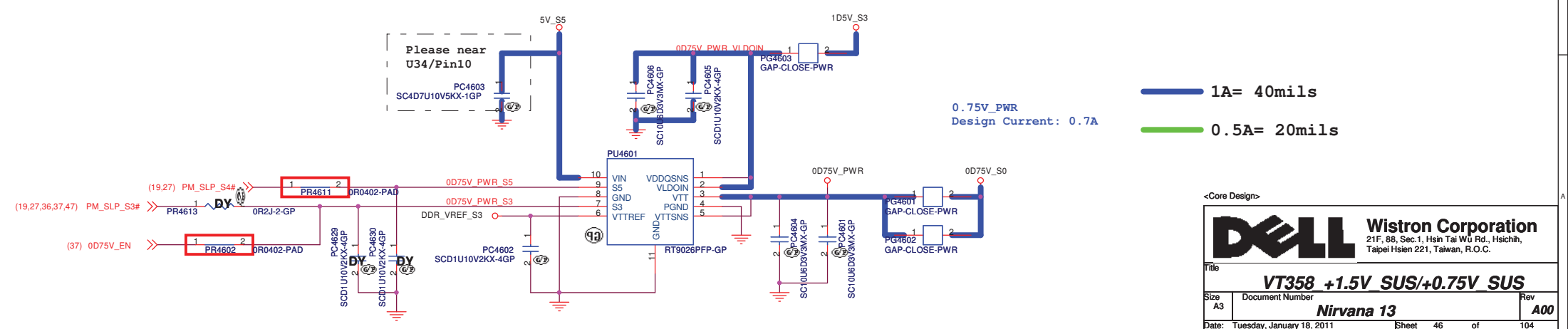
```
SSID = CPU.Regulator
```



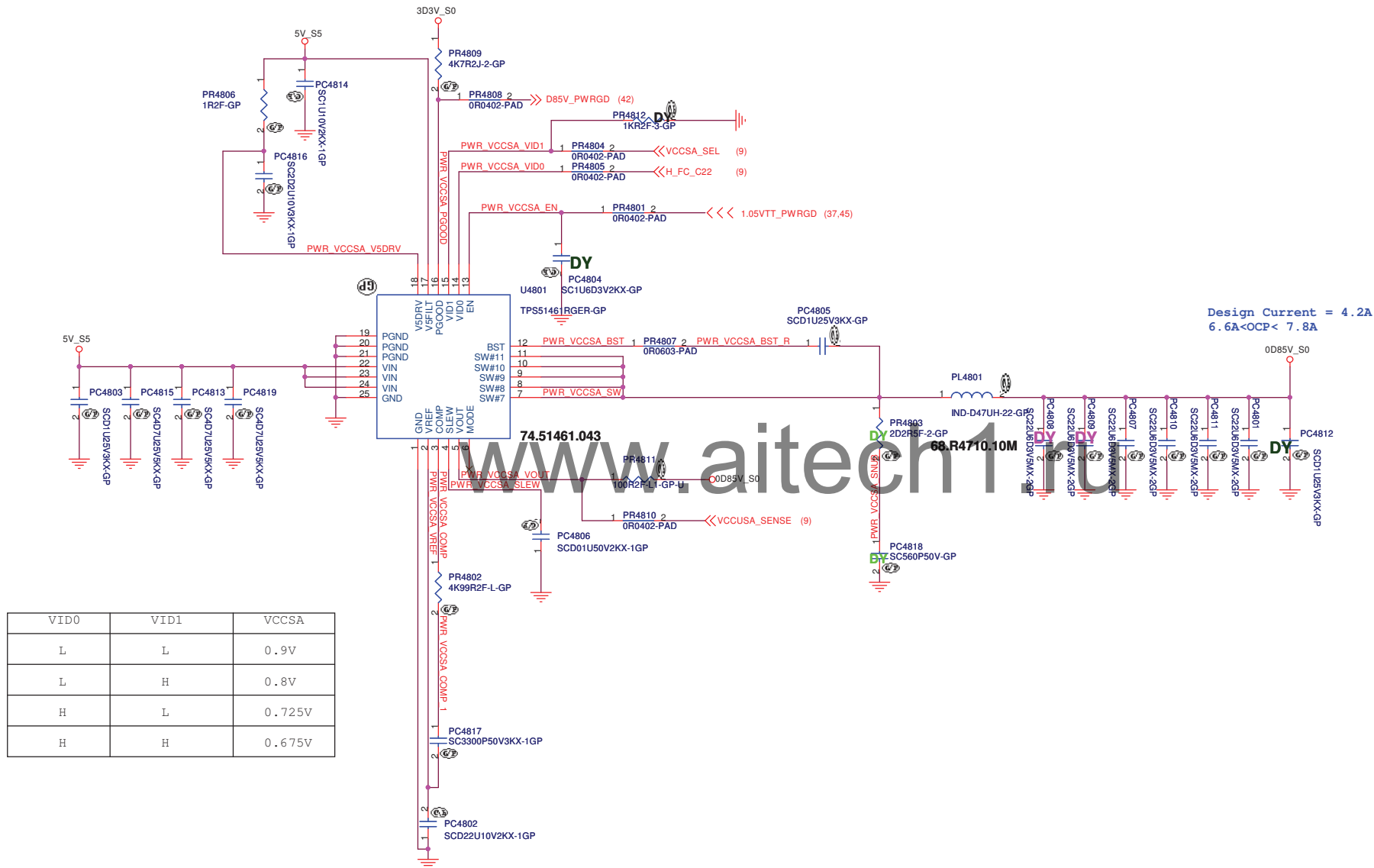
SSID = PWR.Plane.Regulator_1p5v0p75v



RT9026 for 0D75V_S0



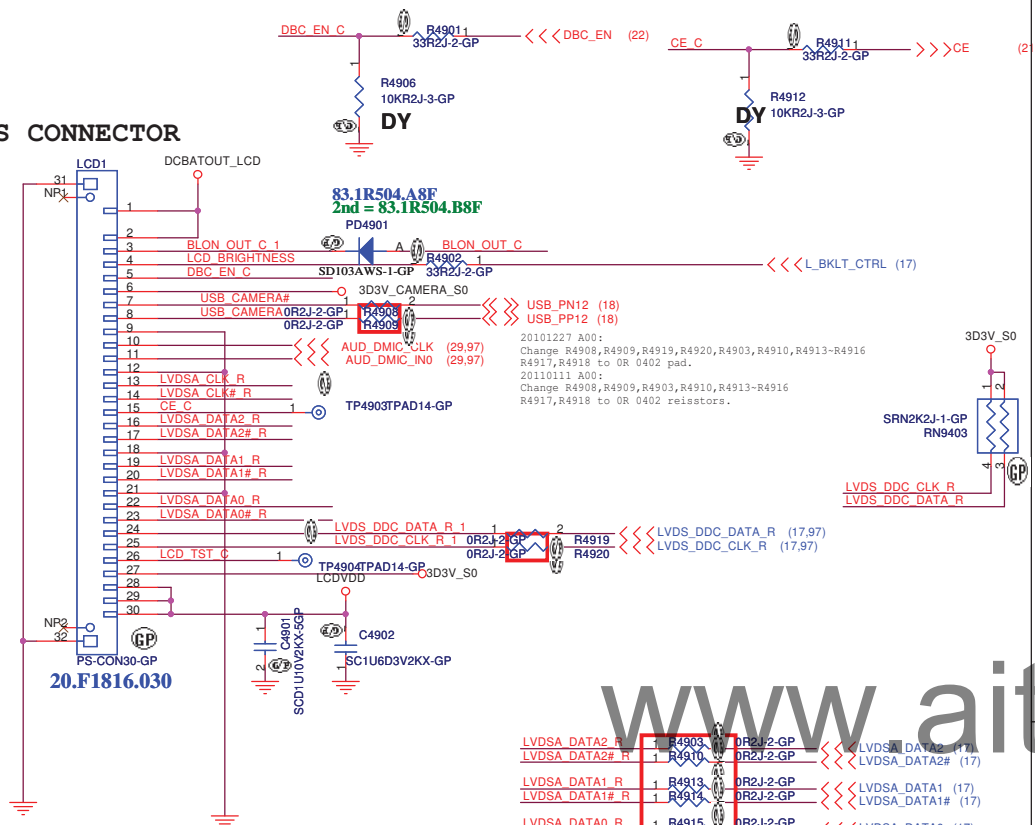
TPS51461 for VCCSA



<Core Design>

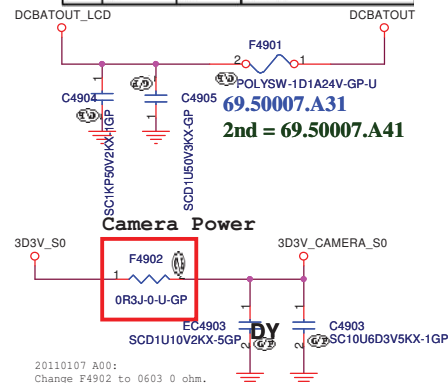
SSID = VIDEO

LVDS CONNECTOR

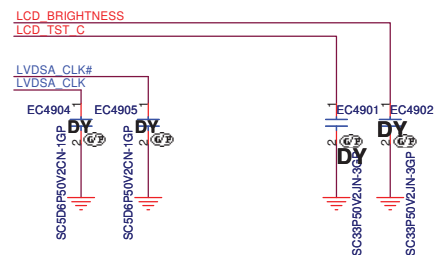


CAMERA and DIGITAL MIC PIN DEFINE!

Pin No.	Name	Pin Type	Function Description
1	diag_sclp	FWO	Calvin Connection Selection
2	daa	Data Pin	USB Data Information
3	di	Data Pin	USB Data Information
4	vib+3.3v	Power Pin	Power Supply
5	DMC_CLK	Data Pin	Digital MIC CLOCK
6	DMC_SND	SND	Digital MIC SND
7	DMC_DATA	Data Pin	Digital MIC DATA
8	SND	SND	Speakers Ground

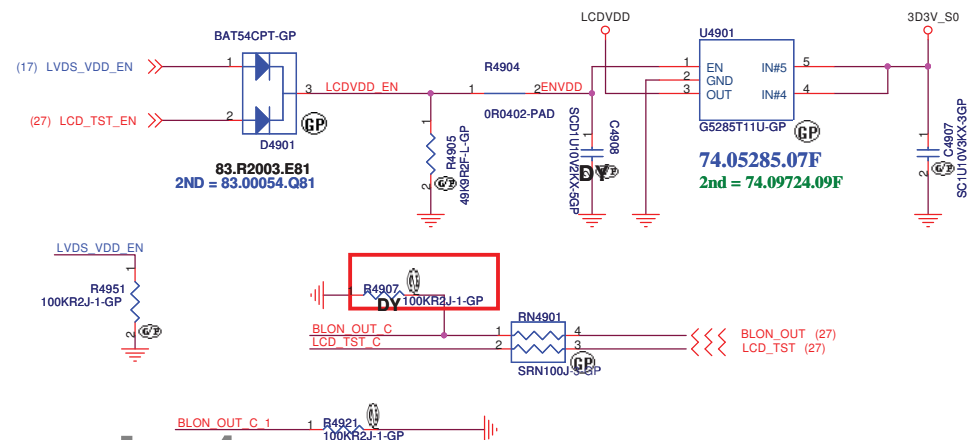


For EMI request
Close to LVDS connector



SSID = VIDEO

LCD POWER for ROSA



20100104 A00:
Remove TR4902.

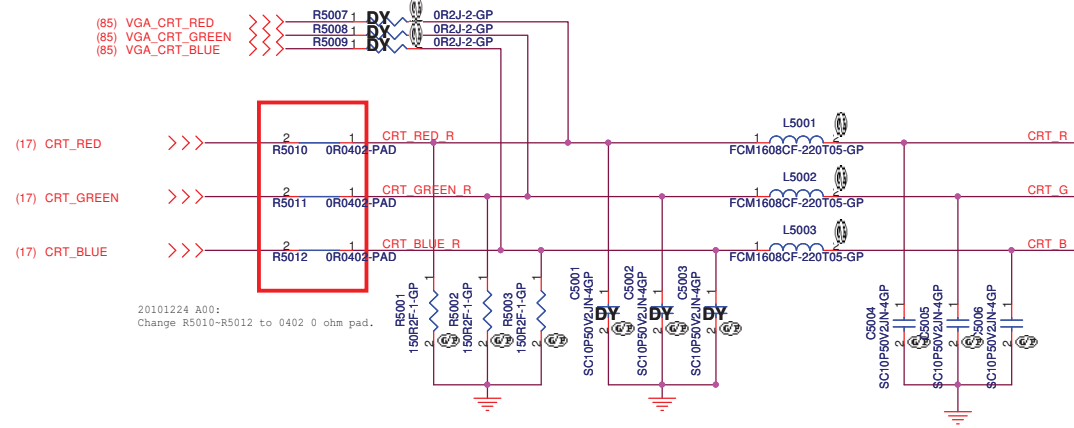
<Core Design>



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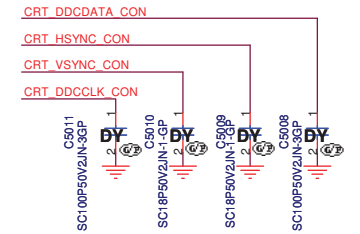
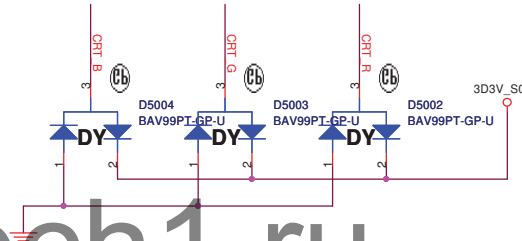
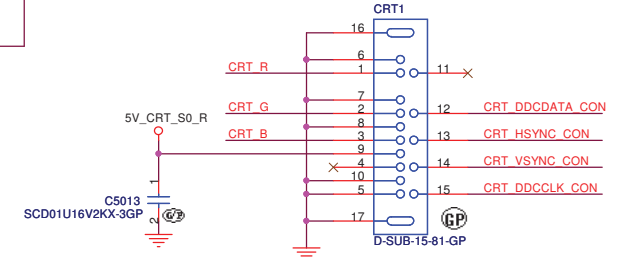
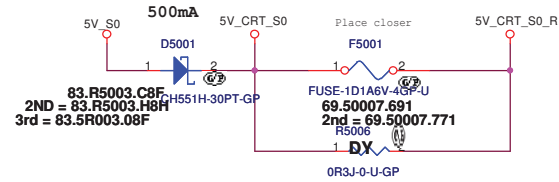
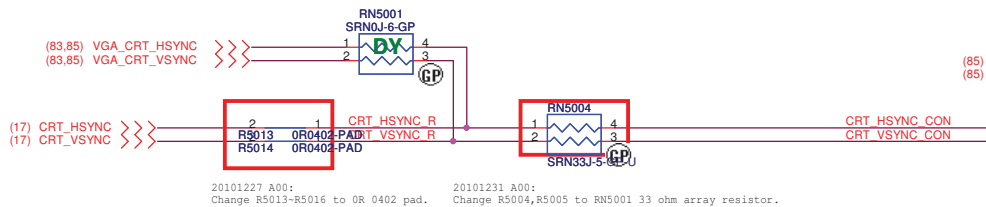
Title			
LCD/Inverter Connector			
Size A3	Document Number		Rev
	Nirvana 13		A00
Date:	Tuesday, January 18, 2011	Sheet 49 of	104

Reserve for ATI to debug



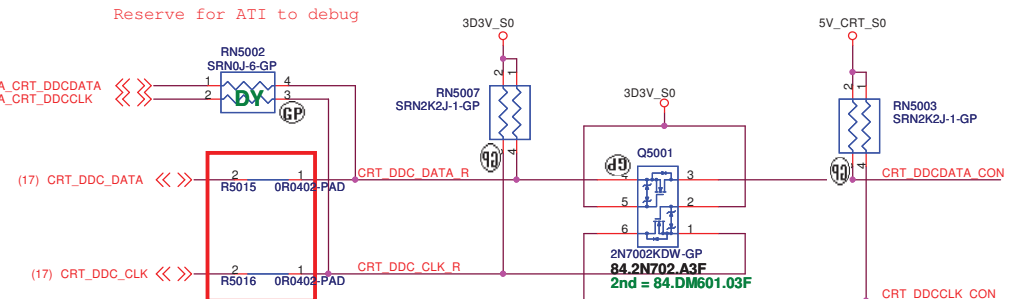
Reduce layout branch trace.
Keep reserved component near main signal

CRT Hsync & Vsync level shift



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CRT DDCDATA & DDCCLK level shift



<Core Design>

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Title			CRT Connector	
Size	Document Number	Rev		A00
A3	Nirvana 13			
Date:	Tuesday, January 18, 2011	Sheet	50	of 104

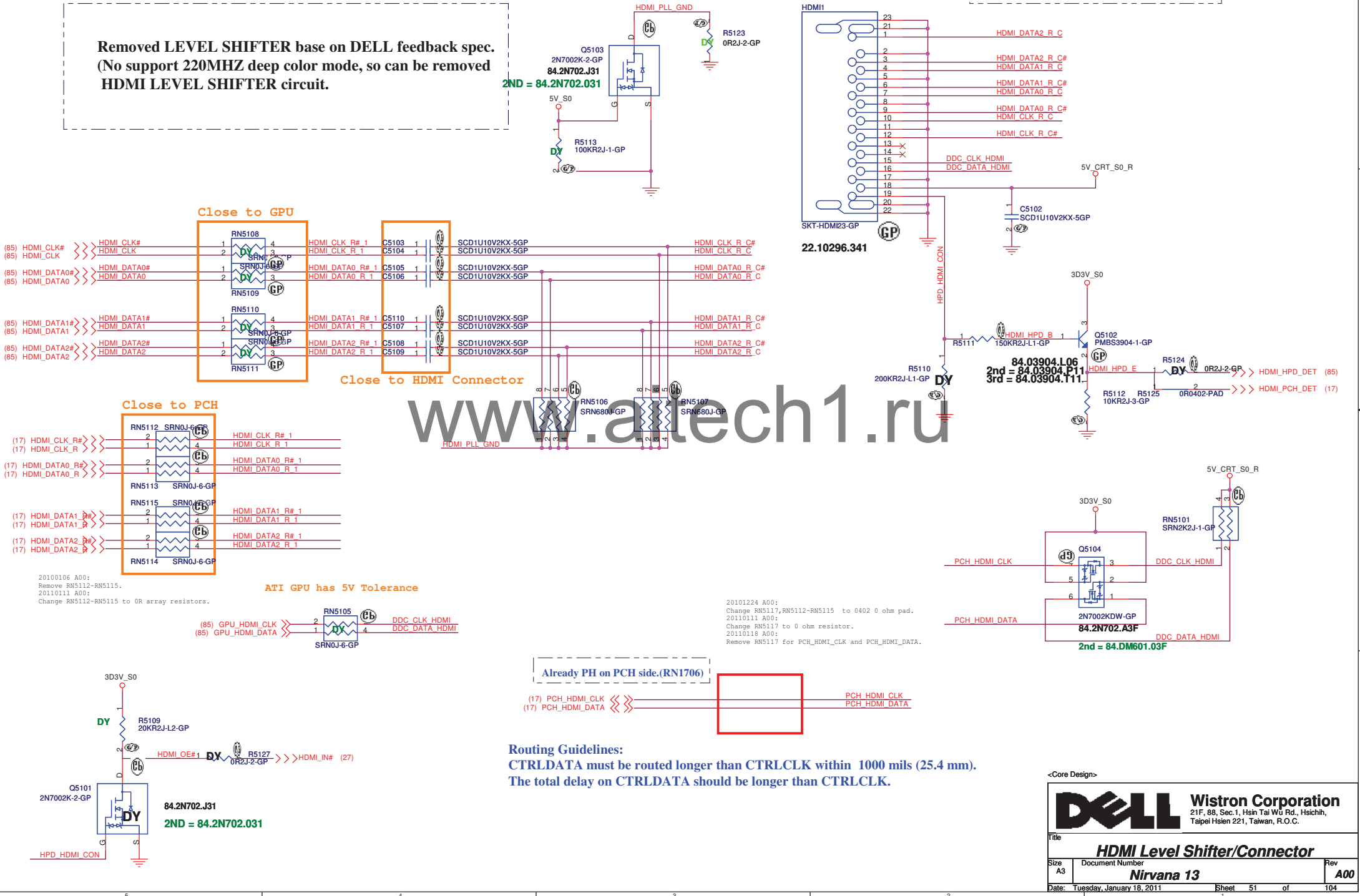
SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Removed LEVEL SHIFTER base on DELL feedback spec.
(No support 220MHZ deep color mode, so can be removed
HDMI LEVEL SHIFTER circuit.

HDMI CONN


Removed HDMI_IN# CIRCUIT
connect to KBC GPIO.



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Title

Reserved

Size
A3

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<Core Design>



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Title

LVDS Switch

Size
A3

Document Number

Nirvana 13

Rev

A00


Date: Tuesday, January 04, 2011

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Title

Reserved

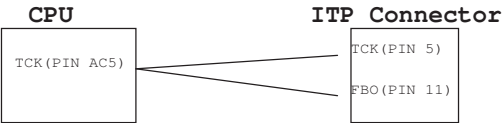
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SSID = User.Interface

ITP Connector

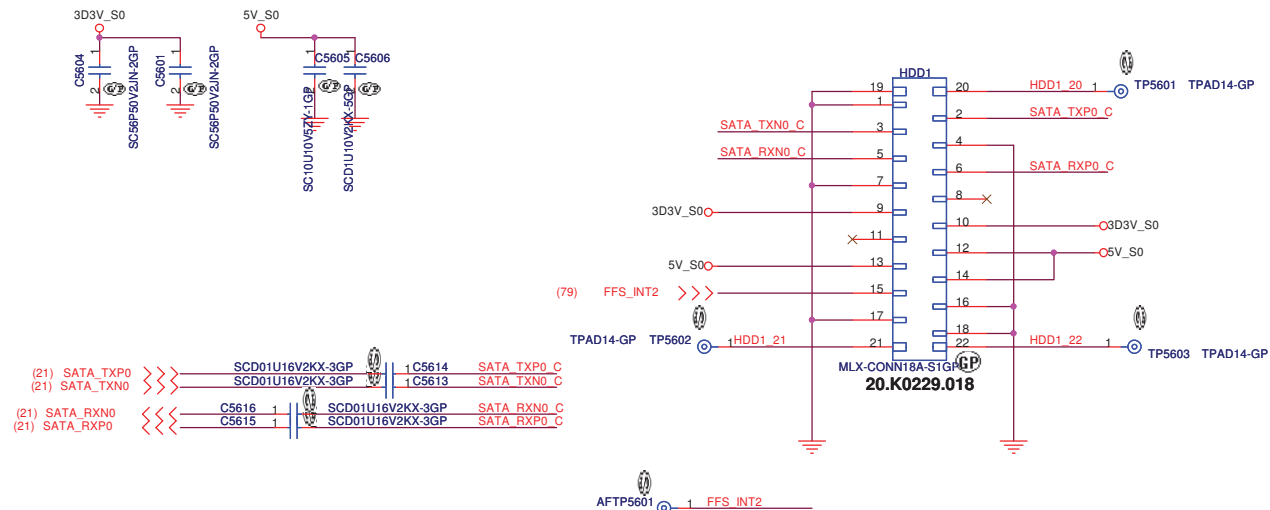
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



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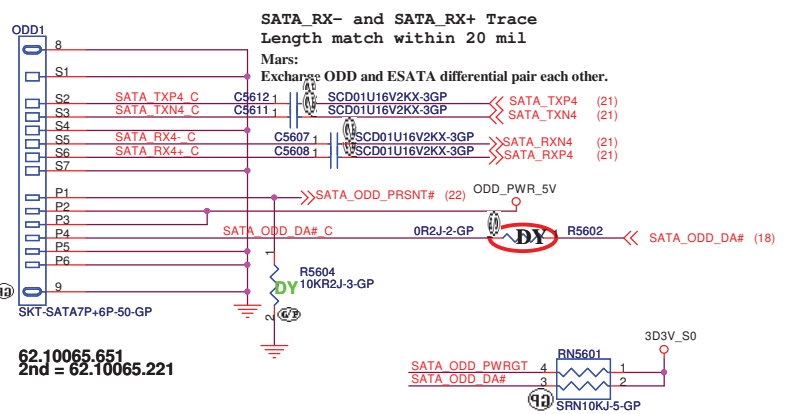
SSID = SATA

SATA HDD Connector

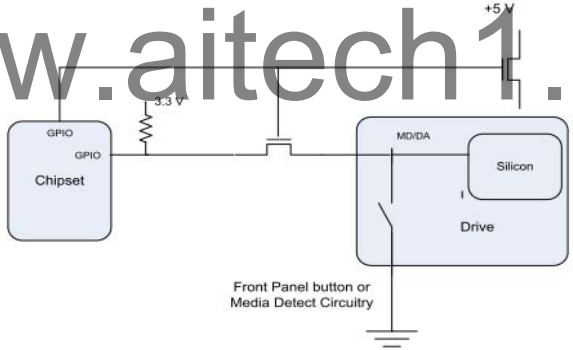


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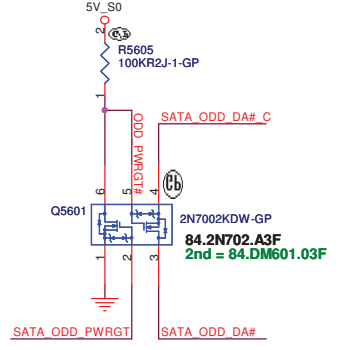
ODD Connector



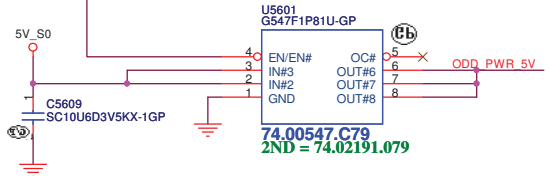
SUPPORT ZERO SATA ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SATA Zero Power ODD



Current limit
Active High
typ =>2A

<Core Design>

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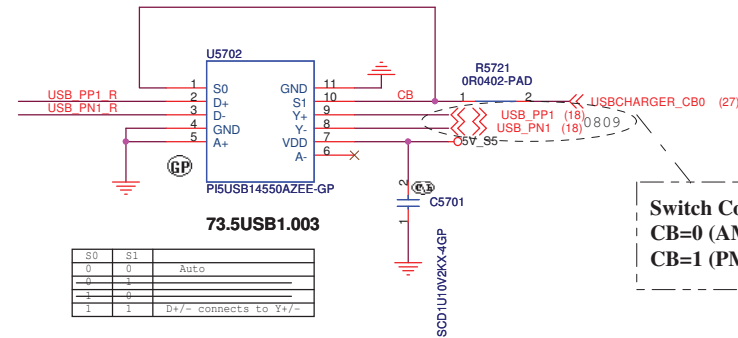
Title: **HDD/ODD**

Size: A3 Document Number: **Nirvana 13** Rev: **A00**

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SSID = ESATA

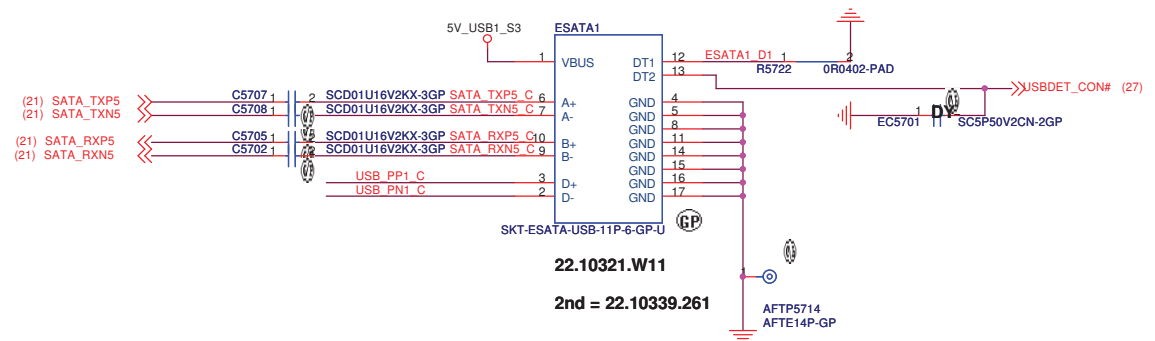
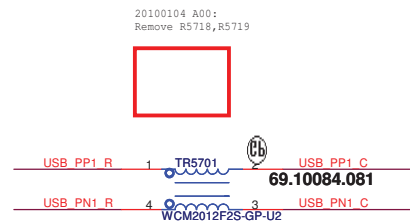
USB CHARGER



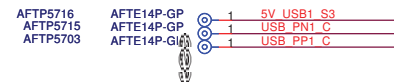
Switch Control Bit:
CB=0 (AM):auto detection charger identification active.
CB=1 (PM):connect DP/DM to TDP/TDM.

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ESATA CONN



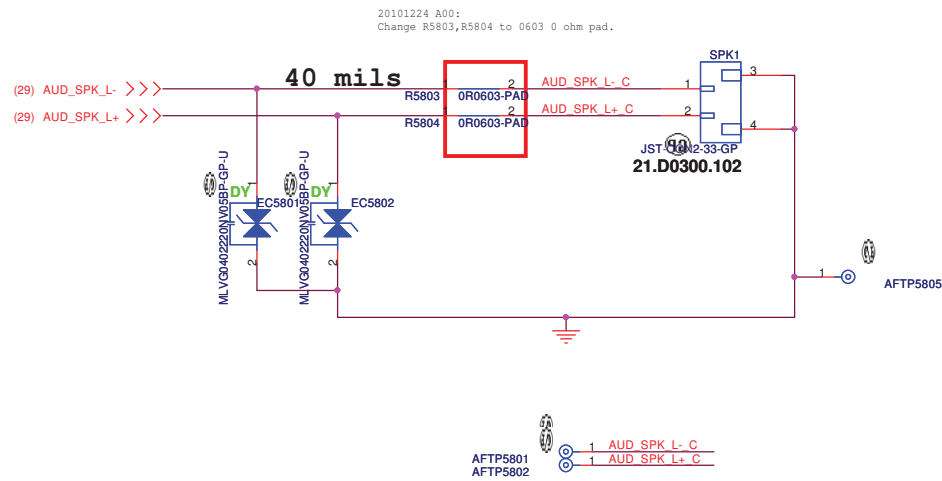
close to ESATA1



<Core Design>

SSID = AUDIO

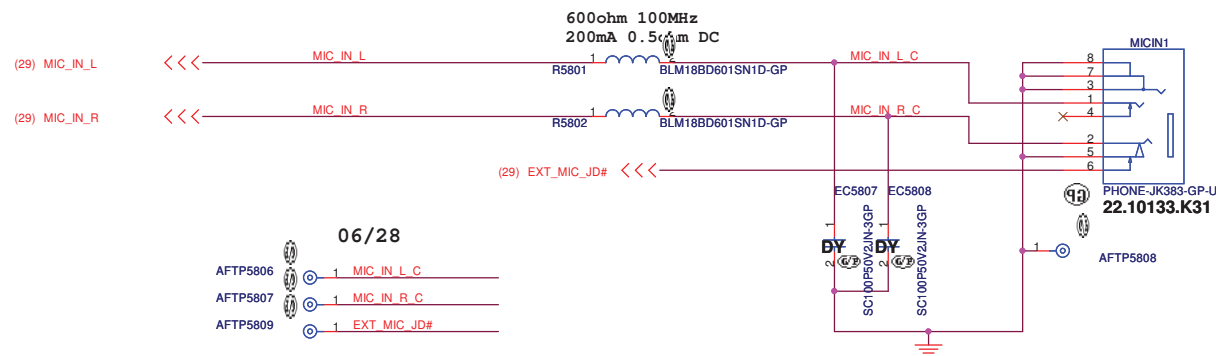
Speaker Connector



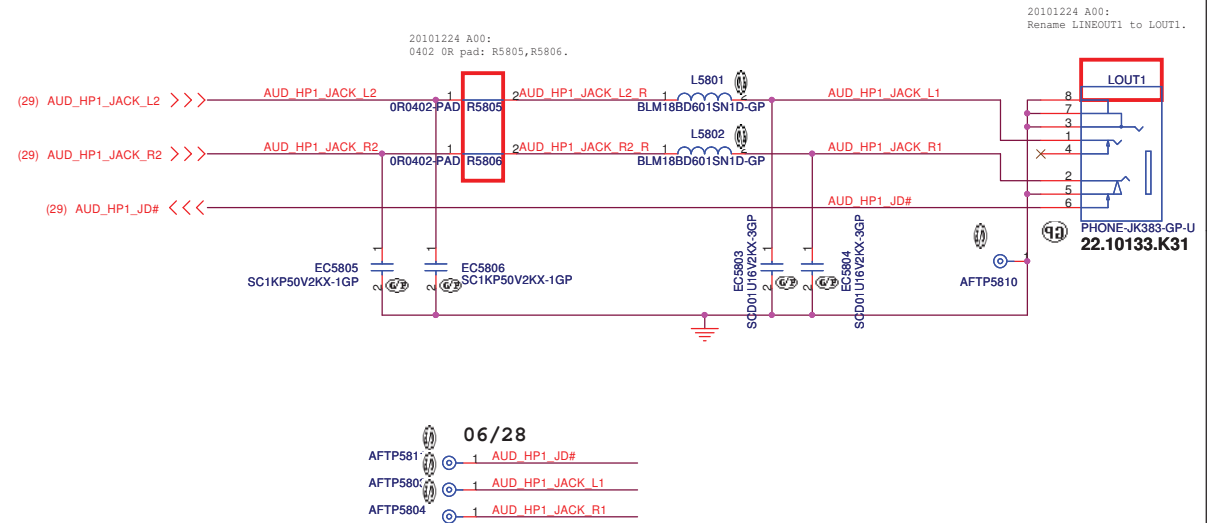
06/28

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MIC IN



LINE OUT



<Core Design>

(Blanking)

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<Core Design>

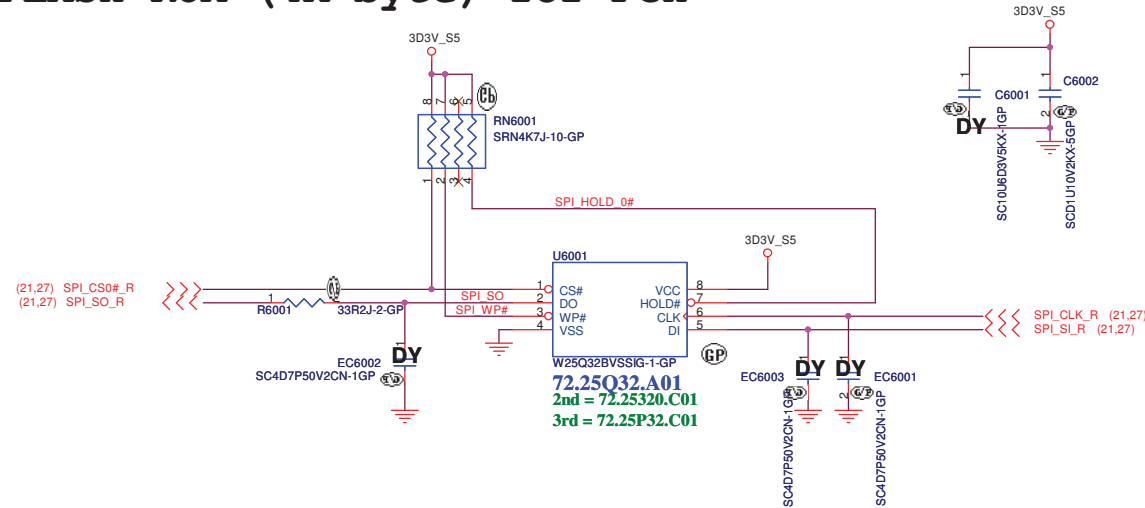


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Title			Reserved		
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SSID = Flash.ROM

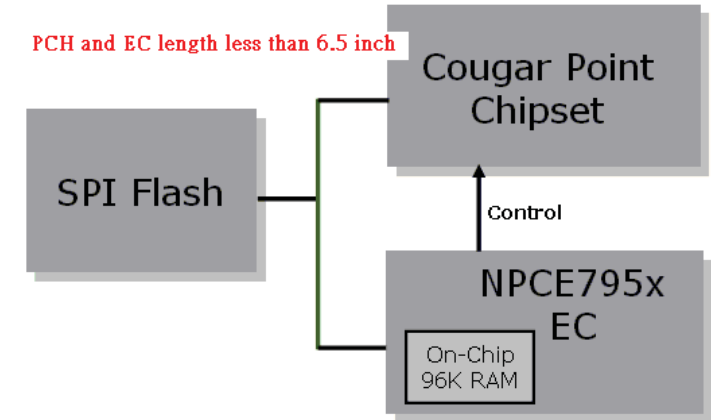
SPI FLASH ROM (4M byte) for PCH



Notes:

The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

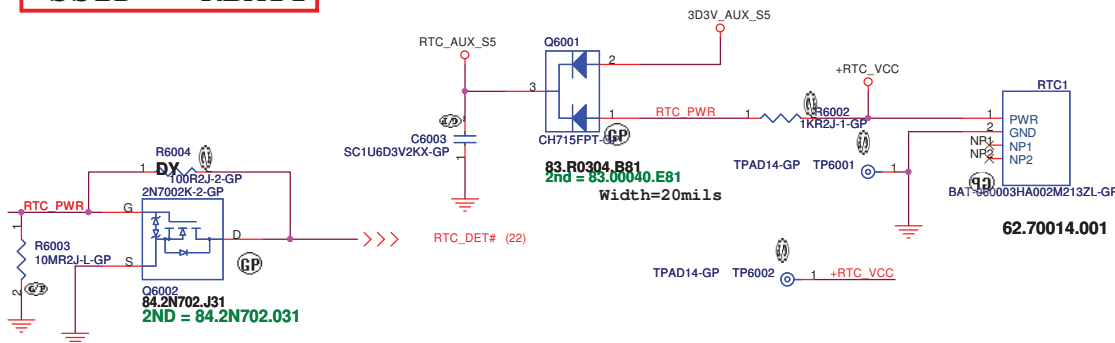
PCH and EC length less than 6.5 inch



Priority	Wistron P/N	Manufacturer	Vendor P/N
1	72.25Q32.A01	WINBOND	W25Q32BVSSIG-1-GP
2	72.25320.C01	MAXIM	MAX3206EM2E-12G
3	72.25P32.C01	NUMONYX	W25P32-VMW6P

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SSID = RBATT

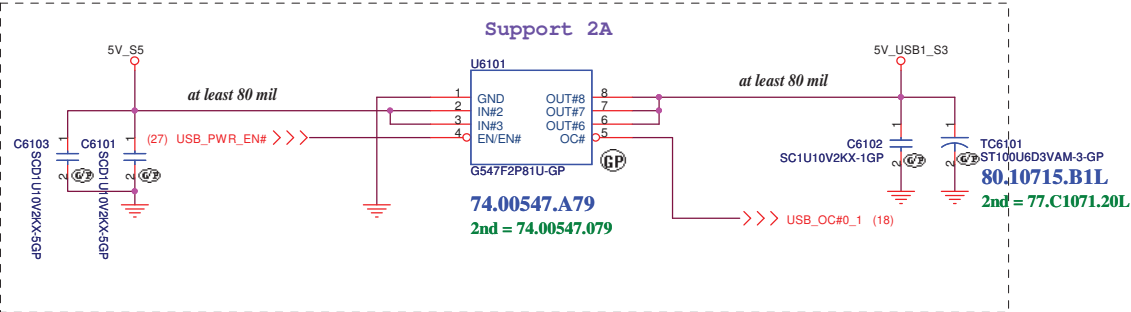


<Core Design>

SSID = USB

Close to ESATA Combo connector

USB POWER SW
Main G547F2P81U-GP P/N:74.00547.A79



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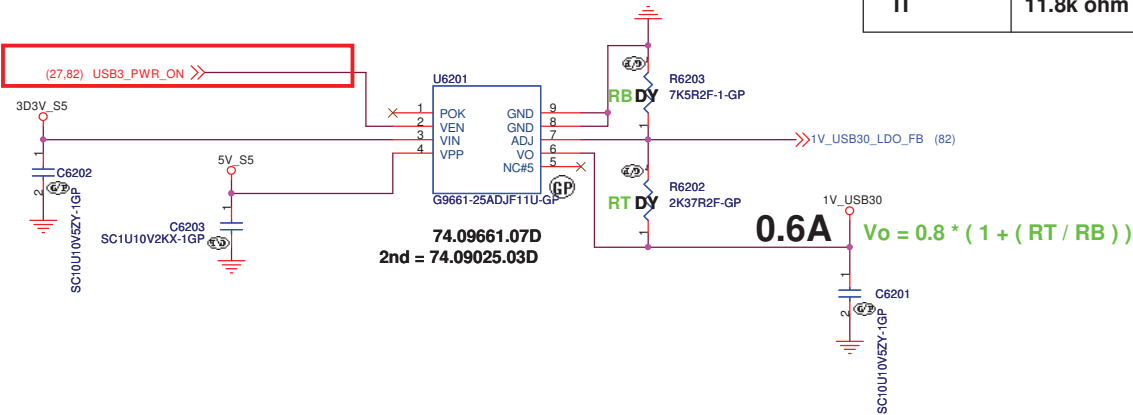
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Title				
USB2.0 Power SW				
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1V_USB30 LDO

20101227 A00:
Change R6205 to 0R 0402 pad.
20101228 A00:
VGA_THERM change to USB_PWR_EN.
20101229 A00:
Remove R6205,R6201 and rename USB3_PWR_ON from USB_PWR_EN.

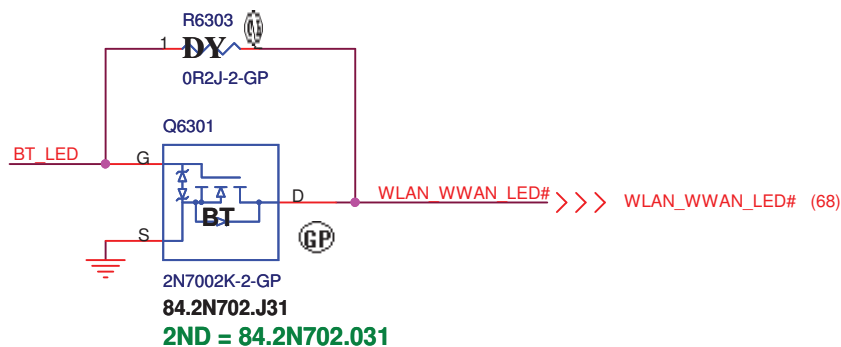
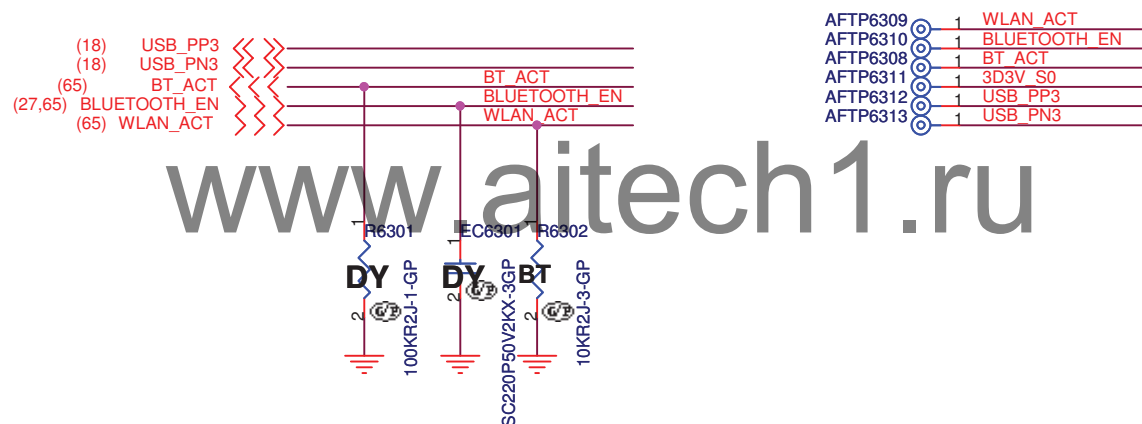
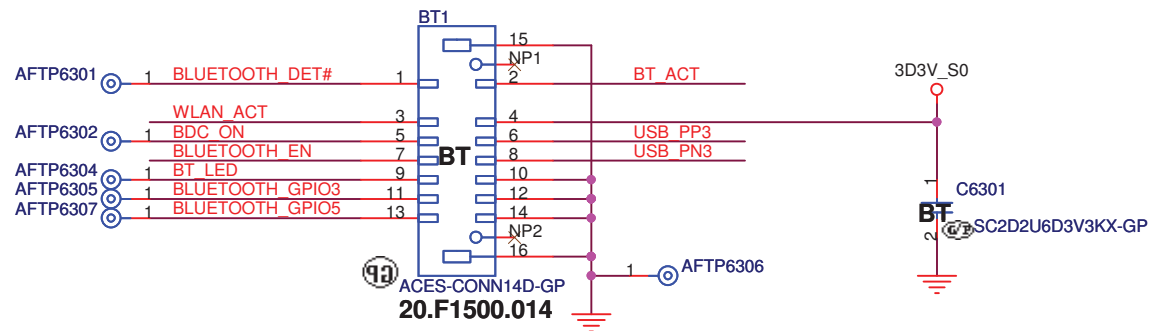
USB3.0 Host	RT (R6202)	RB (R6203)	VOUT
NEC	2.37k ohm (64.23715.6DL)	7.5k ohm (64.75015.6DL)	1.05V
TI	11.8k ohm (64.11825.6DL)	30.9k ohm (64.30925.6DL)	1.1V



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SSID = User.Interface

Bluetooth Module



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Title

Bluetooth

Size
A4

Document Number

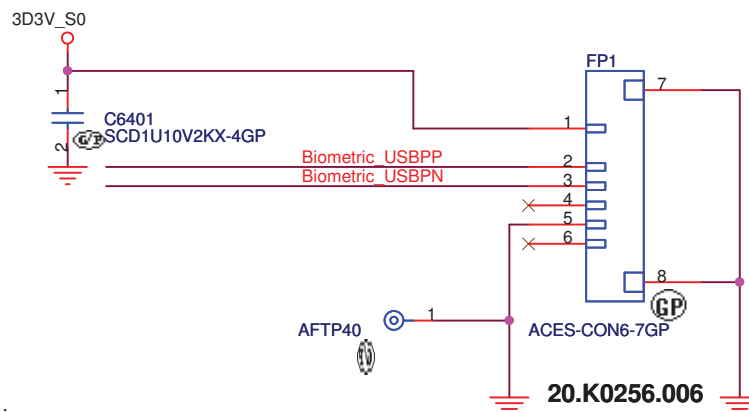
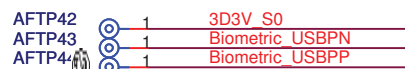
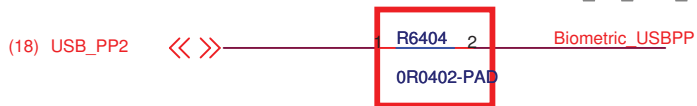
Nirvana 13

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20101227 A00:
Change R6403,R6404 to 0R 0402 pad.
20100104 A00:
Remove TR6401.



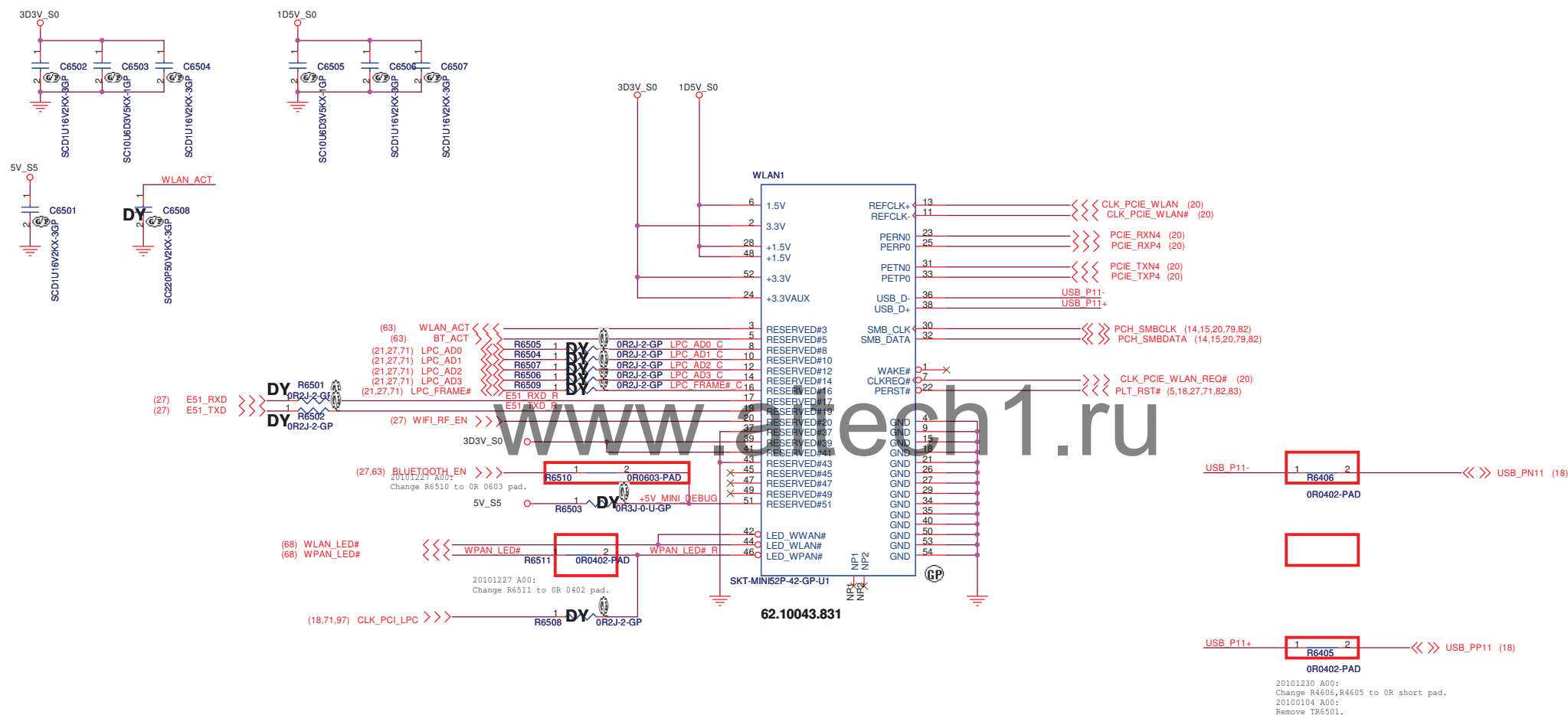
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Finger Printer Conn			
Size A4	Document Number Nirvana 13		Rev A00
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SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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Title

MINICARD(WLAN)/ITP CONN

Size

Document Number

A3

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Title

Size
A3

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Nirvana 13

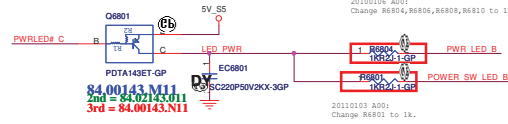
Rev
A00

Date: Tuesday, January 04, 2011

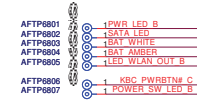
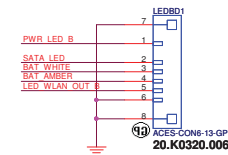
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SSID = User.Interface

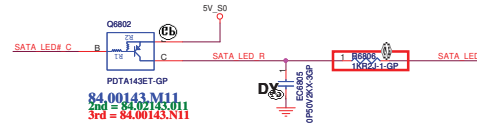
Power LED(White)



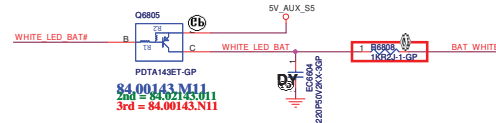
LED BD Connector



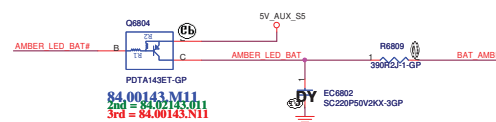
SATA HDD LED(White)



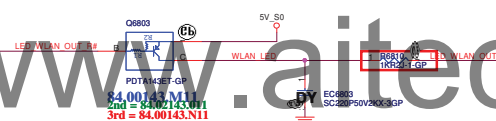
Battery LED1(White)



Battery LED2 (Amber)

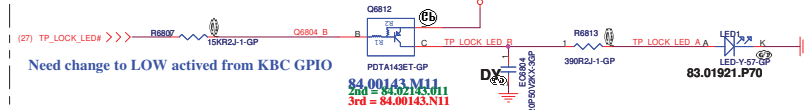


WLAN LED (White)

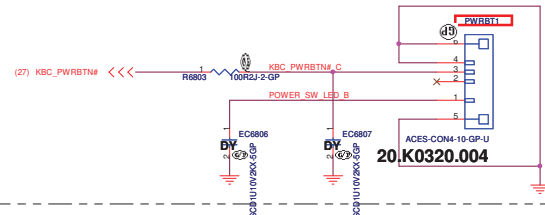


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TPLOCK LED



Power button LED(White)

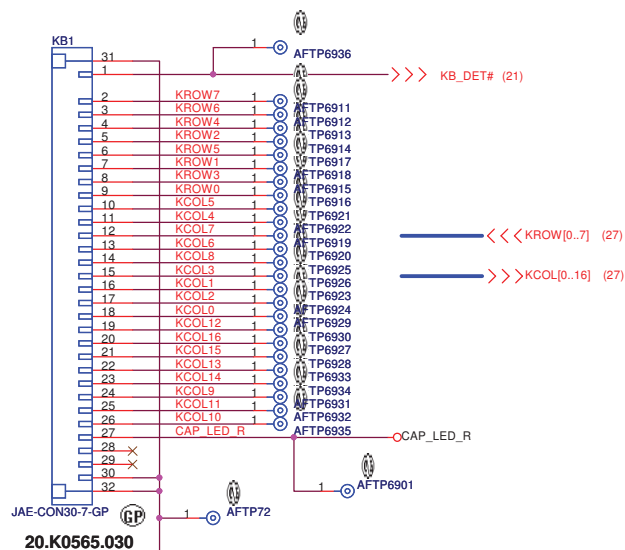


<Core Design>

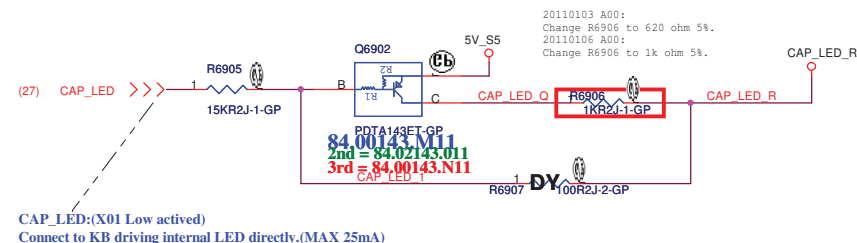
SSID = KBC

Internal KeyBoard Connector

PIN No.	Description
1	Diag_Loop=GPIO_1(TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND



CAP LED CONTROL

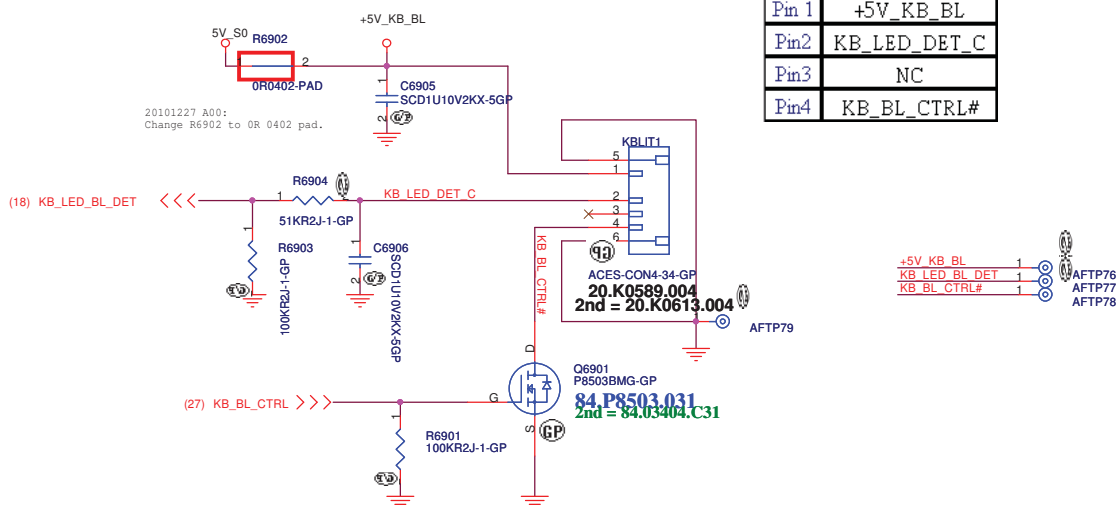


TouchPad LOCKED

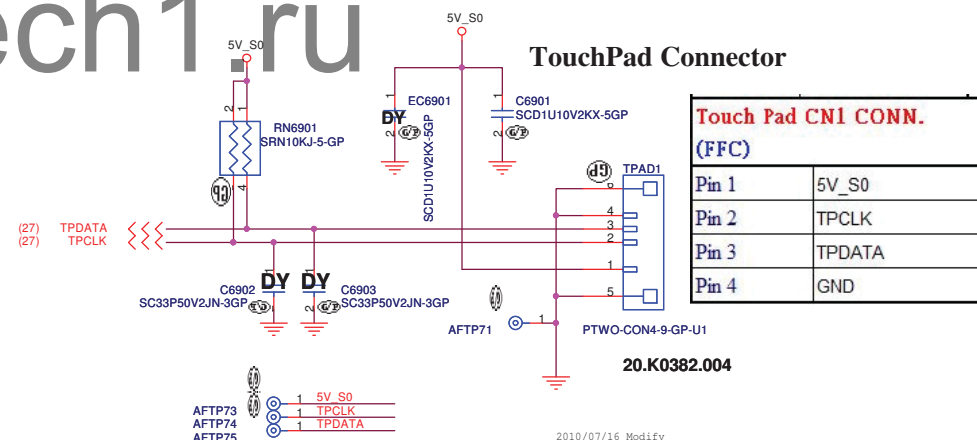
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KB Backlight Connector

MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#



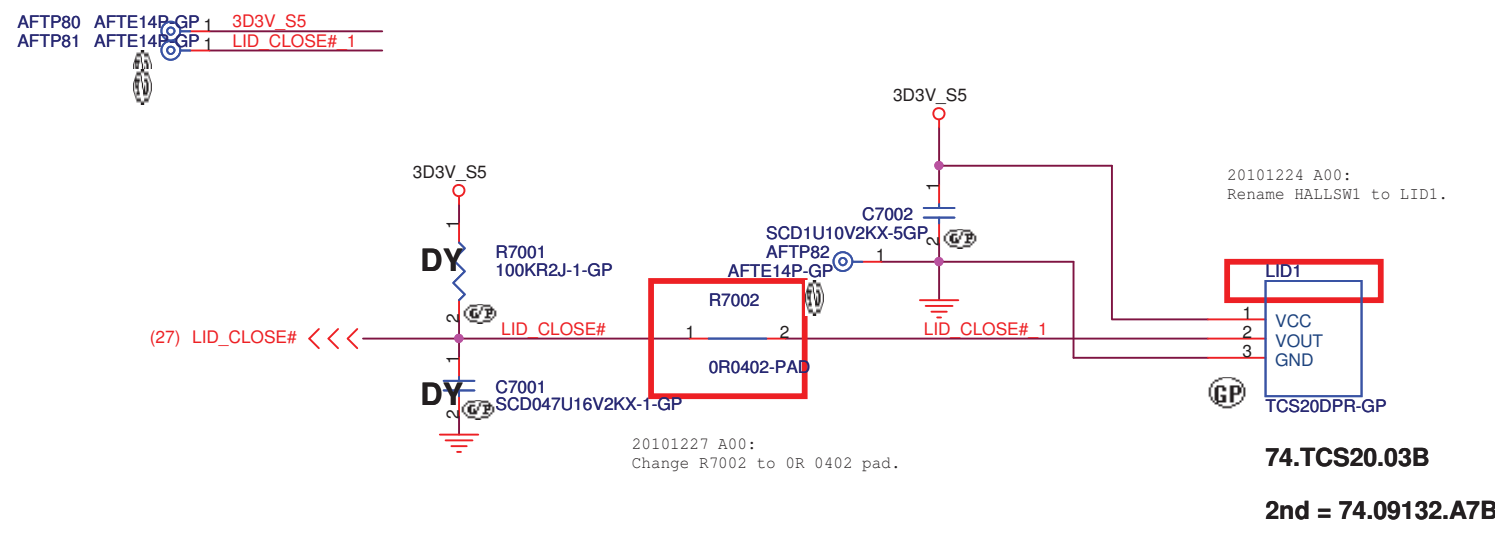
TouchPad Connector



<Core Design>


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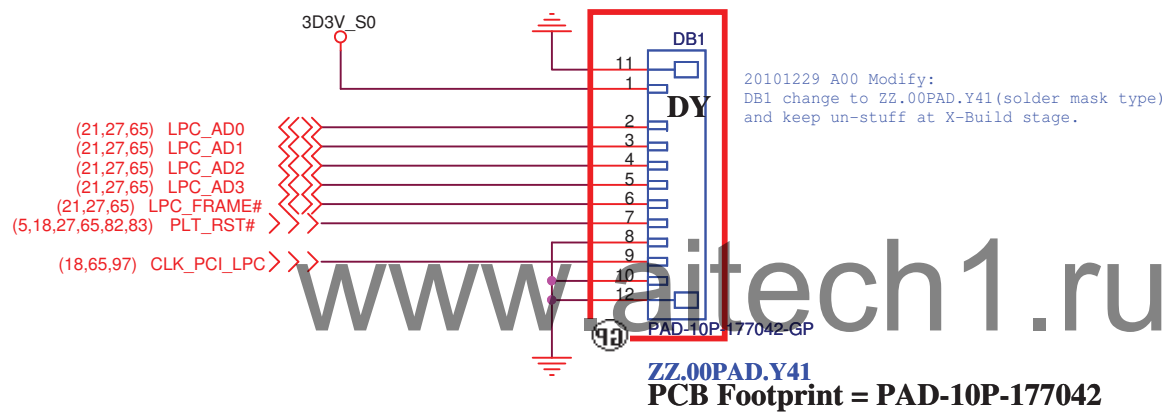
Key Board/Touch Pad/Media Board
Nirvana 13
Date: Tuesday, January 18, 2011 Sheet 69 of 104




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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Hall Sensor			
Size A4	Document Number Nirvana 13		Rev A00
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Dubug CONN	
Title	Dubug CONN		
Size A4	Document Number Nirvana 13	Rev A00	
Date: Tuesday, January 18, 2011	Sheet 71 of 104		

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Title

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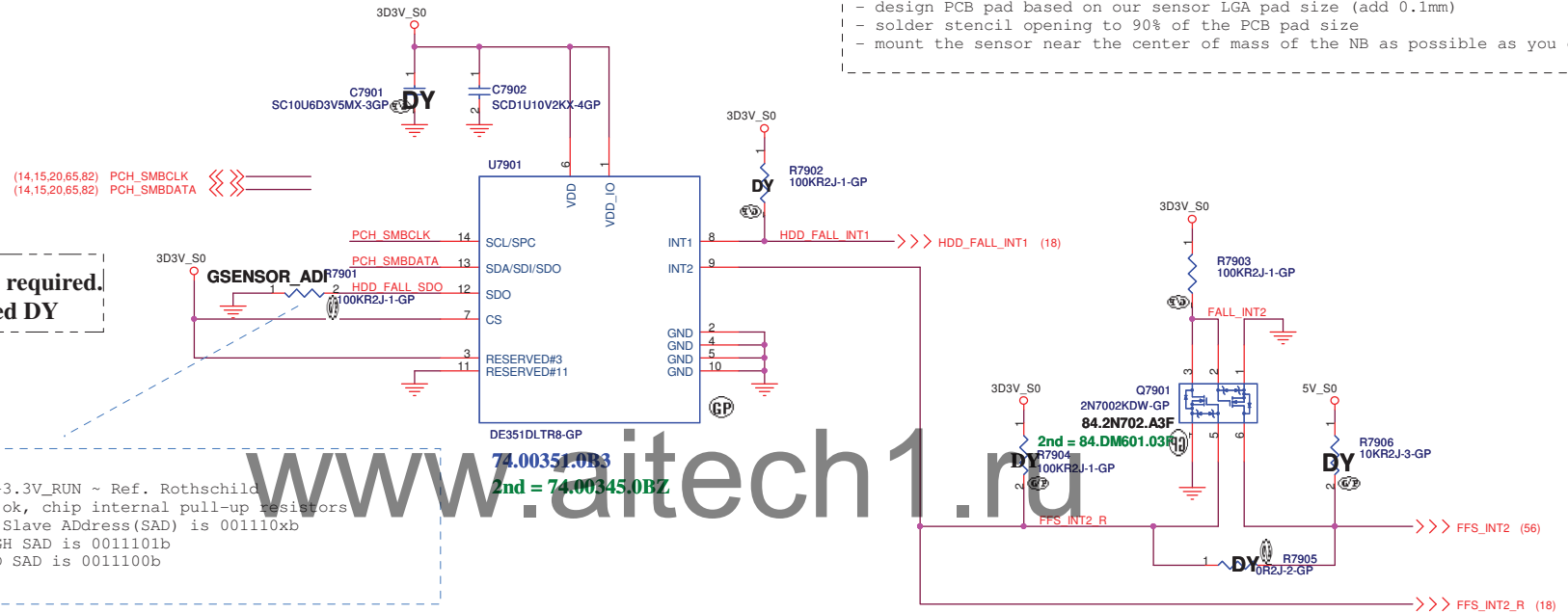
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```
SSID = User.Interface
```

Free Fall Sensor

| Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



For ADI G-sensor : R7901 is required.
For ST G-sensor : R7901 need DY

```
09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave Address(SAD) is 001110xb
    Pull HIGH SAD is 0011101b
    Pull GND SAD is 0011100b
```

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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DELL

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Title	Author	Date	Location	Notes
1	John Doe	1998	New York	First edition
2	Jane Smith	2001	London	Second edition
3	Robert Brown	2005	Paris	Third edition
4	Emily White	2010	Tokyo	Fourth edition
5	Michael Green	2015	Sydney	Fifth edition

Free Fall Sensor

Size
A3

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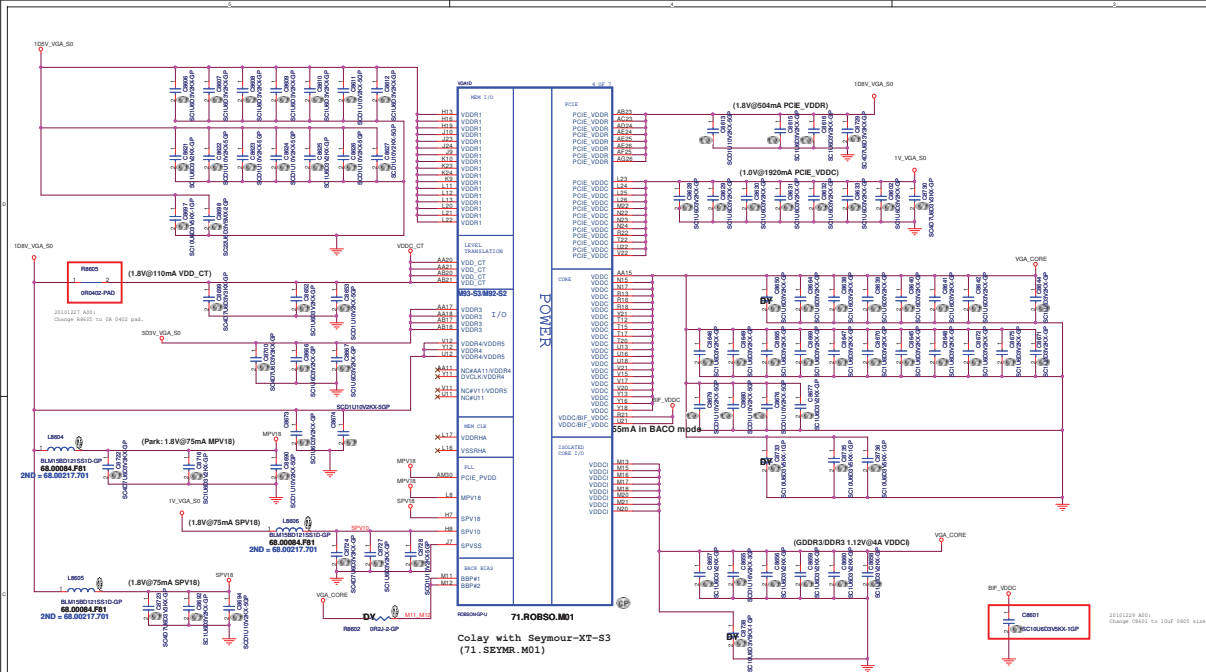
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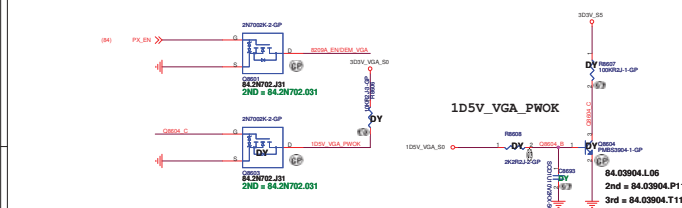
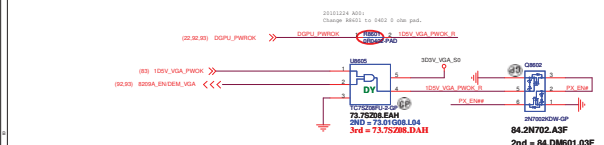
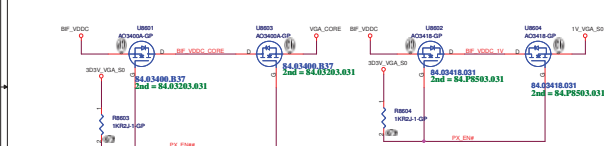
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Title _____			
Size A2		Document Number GPU Memory(2/5)	
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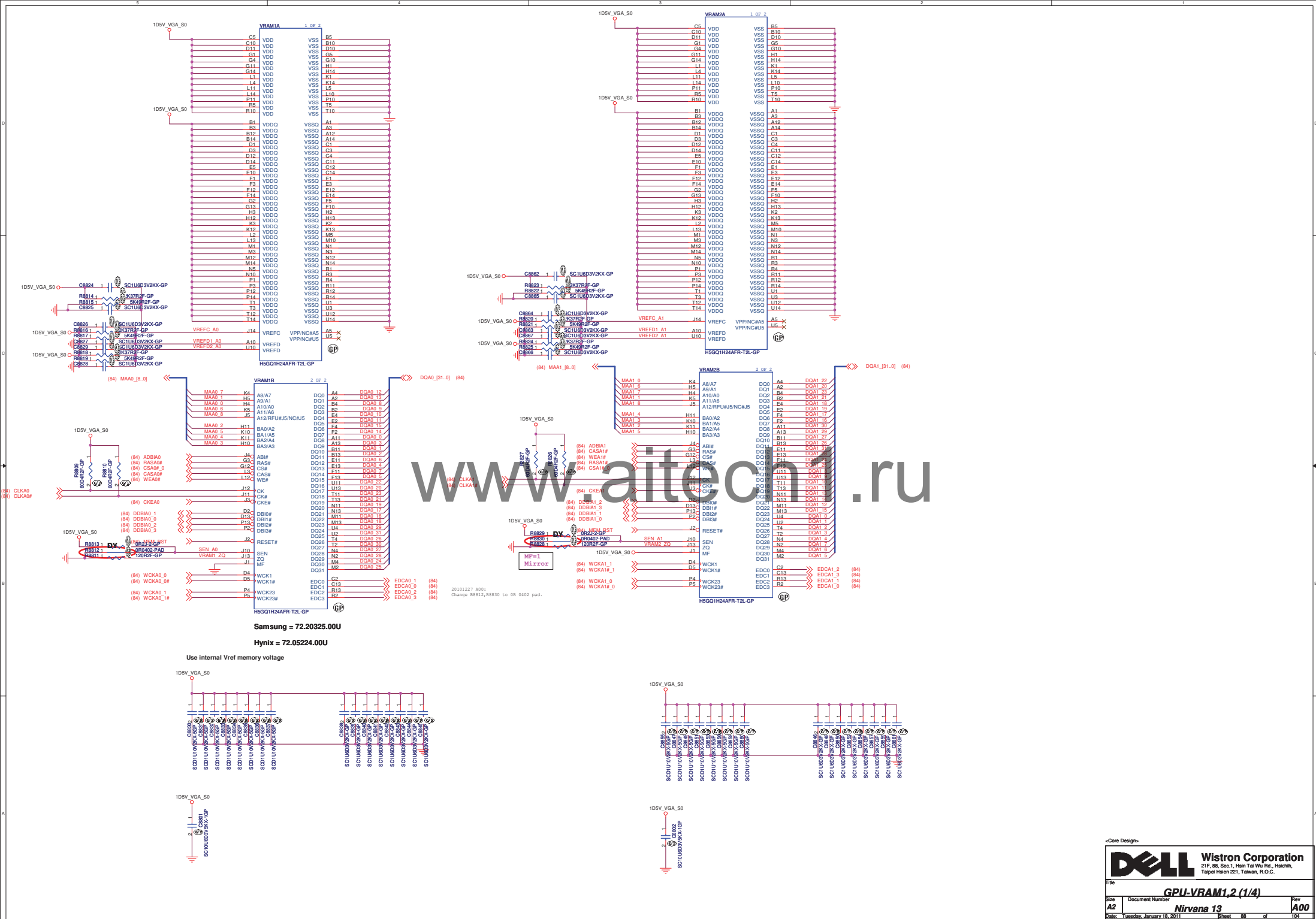
PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

PX_EN	Mode	BIF_VDDC	PX_EN#	Mode	BIF_VDDC	PX_EN#	Mode	BIF_VDDC
0	Normal	VGA_Core	0	Normal	VGA_Core	0	Normal	VGA_Core
1	BACO	1V_VGA	1	BACO	1V_VGA	1	BACO	1V_VGA

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN# = High, BIF_VDDC = VGA_Core




<div>  <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div>			
Title			
GPU DPPWR/GND(5/5)			
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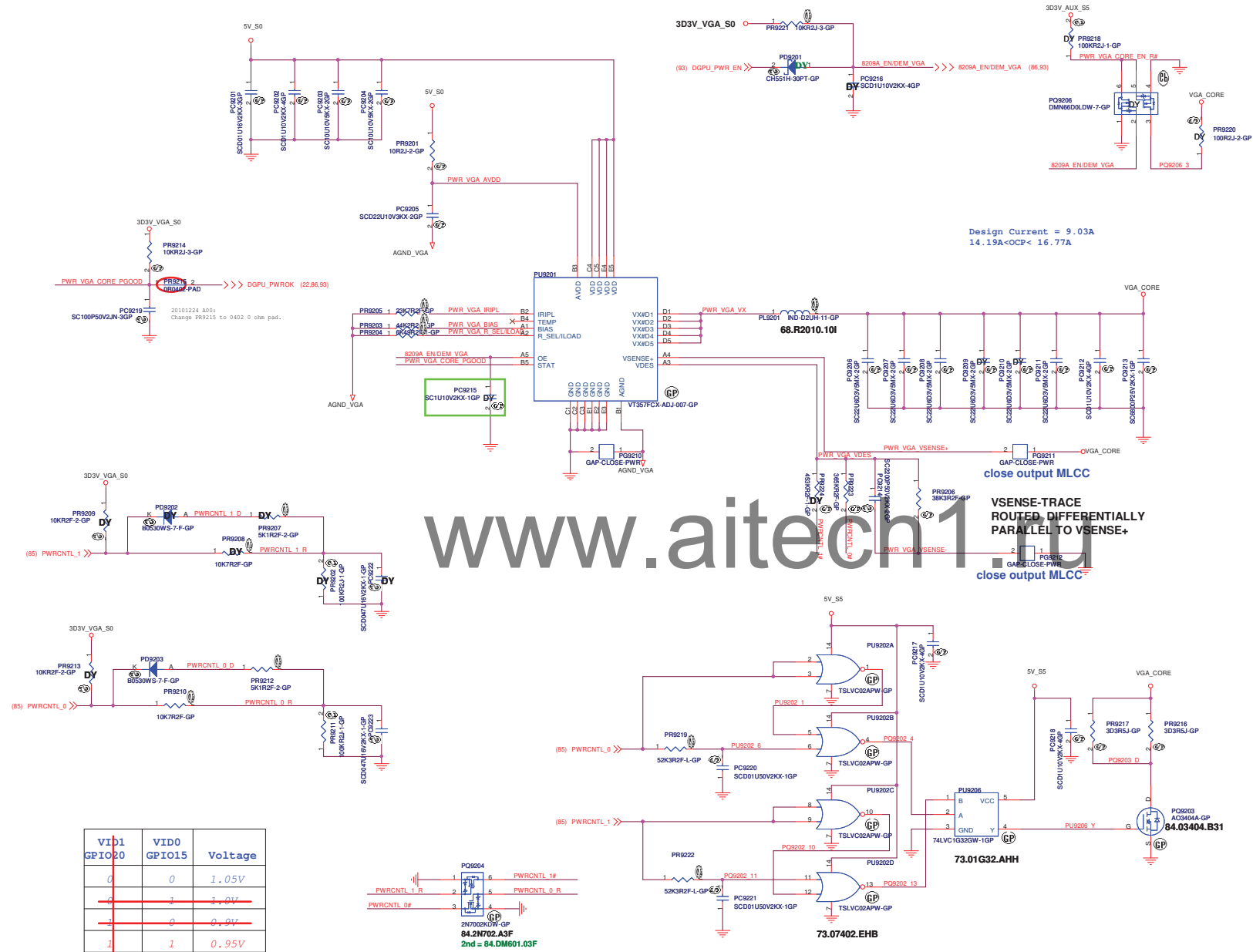
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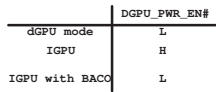


VID1 GPIO20	VID0 GPIO15	Voltage
0	0	1.05V
0	1	1.0V
1	0	0.9V
1	1	0.95V

PR9206	38.3	kohm
PR9224	DY	
PR9223	365	kohm

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20110105 A00:
Change PR9316 to 10k ohm (follow the standard schematics).

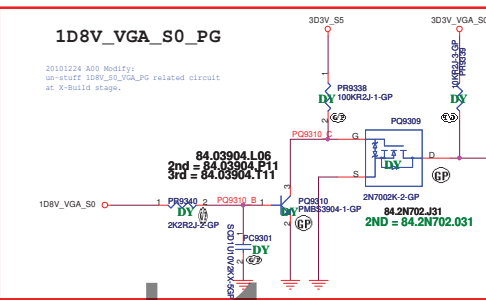


(18) DGPU_PWR_EN# >>> DIS 1D8V VGA_S0

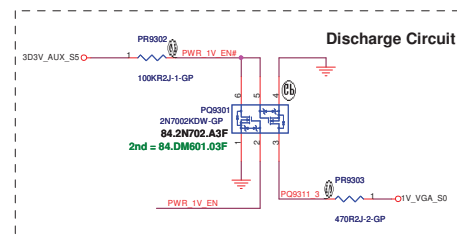
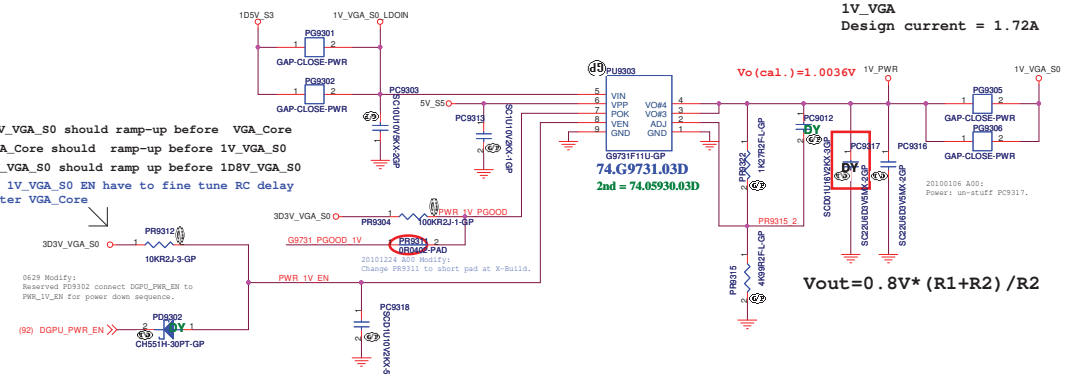
DGPU_PWR_EN
1D8V VGA_EN#
DIS 1D8V VGA_S0

2N7002K.DIF-GP
84.2N702.A3F
2nd = 84.DM601.03F

20101228 A00 Modify:
Change PR9320 to short pad at X-Build.



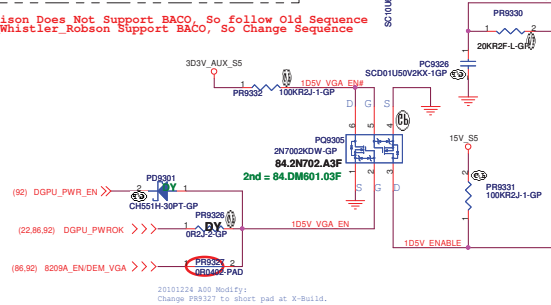
```
3D3V_VGA_S0 should ramp-up before  VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
so 1V_VGA_S0 EN have to fine tune RC delay
after VGA_Core
```



change low $R_{ds(on)}$ MOSFET

1D5V_S3 to 1D5V_VGA_S0 trace need increase to avoid 1D5V_VGA_S0 DROP Voltage.

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence



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(AC mode)

Within logic high level and disable if it is less than the logic low level.

VSRZF_Sus must be powered up before VocRef3_3, or after VocRef3_3 within 0.7 V. Also, VSRZF_Sus must power down after VocRef3_3, or before VocRef3_3 within 0.7 V.

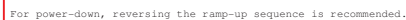
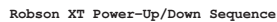
Not floating.

Sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ns de-bounce on the input.

VSREF must be powered up before Voc1_3, or after Voc2_3 within 0.7 V. Also, VSREF must power down after Voc1_3, or before Voc2_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.



red word: KBC GPIO

Sense the power button status

VS9ZF_Sus must be powered up before VocSus1_3, or after VocSus1_3 within 0.7 V. Also, VS9ZF_Sus must power down after VocSus1_3, or before VocSus1_3 within 0.7 V.

V162F must be powered up before Vcc1_3, or after Vcc1_3 within 0.7 V. Also, V162F must power down after Vcc1_3, or before Vcc1_3 within 0.7 V

This signal represents the Power Good for all the non-CORE and non-graphics power rails.



The schematic diagram illustrates the power management system for the Dell Wistron C21F laptop. It shows the power flow from the AC adapter and DC battery through various regulators and switches to the CPU and other components. Key components include the RT8223MGQW DC/DC converter, KBC NPCE795P, Cougar Point EC, Sandy Bridge CPU, and several TPS and RT regulators. The diagram is annotated with callouts for various signals and components, and a large watermark 'www.aitech1.ru' is overlaid.

Power Sources and Initial Regulation:

- AC Adapter in (Page 38):** Provides power to the system.
- DC Battery (Page 39):** Provides power to the system.
- SWITCH (Page 40):** Controls the power flow from the AC adapter and battery.
- BQ24745 Charger (Page 40):** Manages the battery charging process.
- RT8223MGQW DC/DC (3V/5V) (Page 41):** Regulates the input voltage to the system.

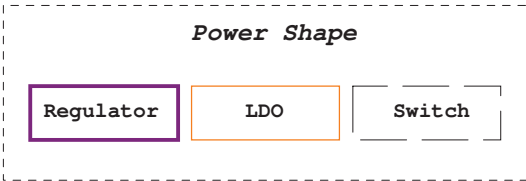
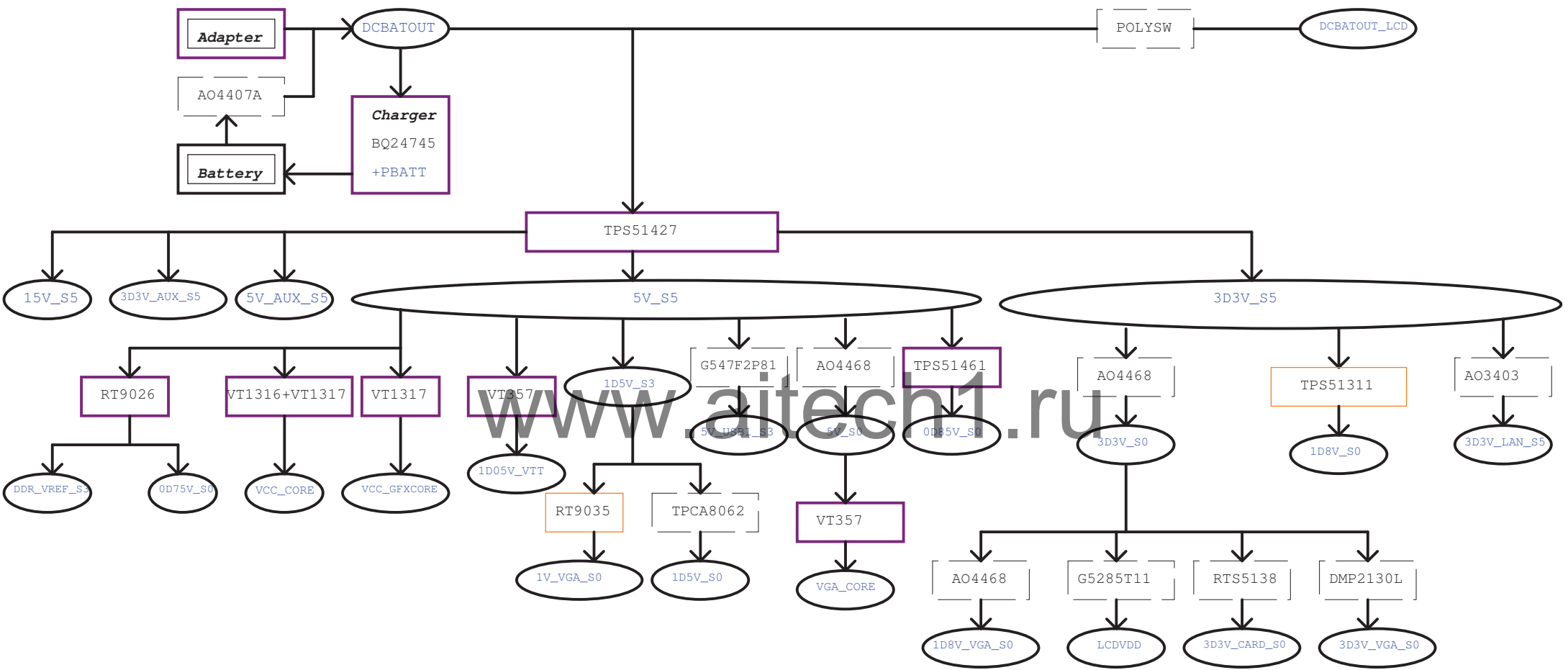
Regulators and Switches:

- TPS51116RGER (Page 46):** Regulates the 1D5V_S3 output.
- TPS53311RGTR (Page 47):** Regulates the 1D8V_S0 output.
- TPS51218DSCR (Page 45):** Regulates the 1D05_VTT output.
- RT8208BGQW (Page 48):** Regulates the 0D85_S0 output.
- ISL95831HRTZ (Page 42 & 43 & 44):** Regulates the VCC_CORE and VCC_GFXCORE outputs.
- RT8223MGQW DC/DC (3V/5V) (Page 41):** Regulates the 5V_S5 and 3D3V_S5 outputs.
- KBC NPCE795P (Page 27):** Controls the system's power states and signals.
- Cougar Point EC (Page 27):** Controls the system's power states and signals.
- Sandy Bridge CPU (Page 27):** The main processor of the system.

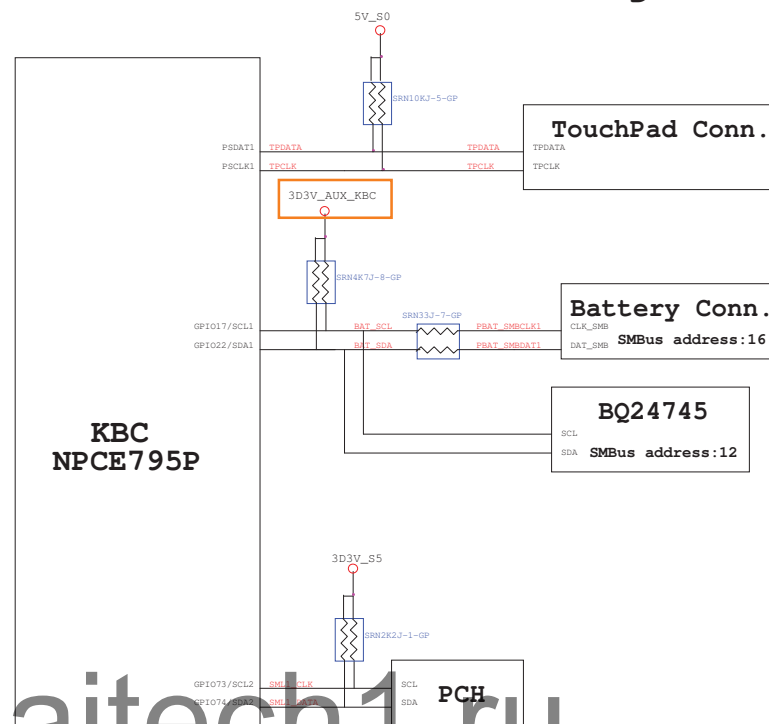
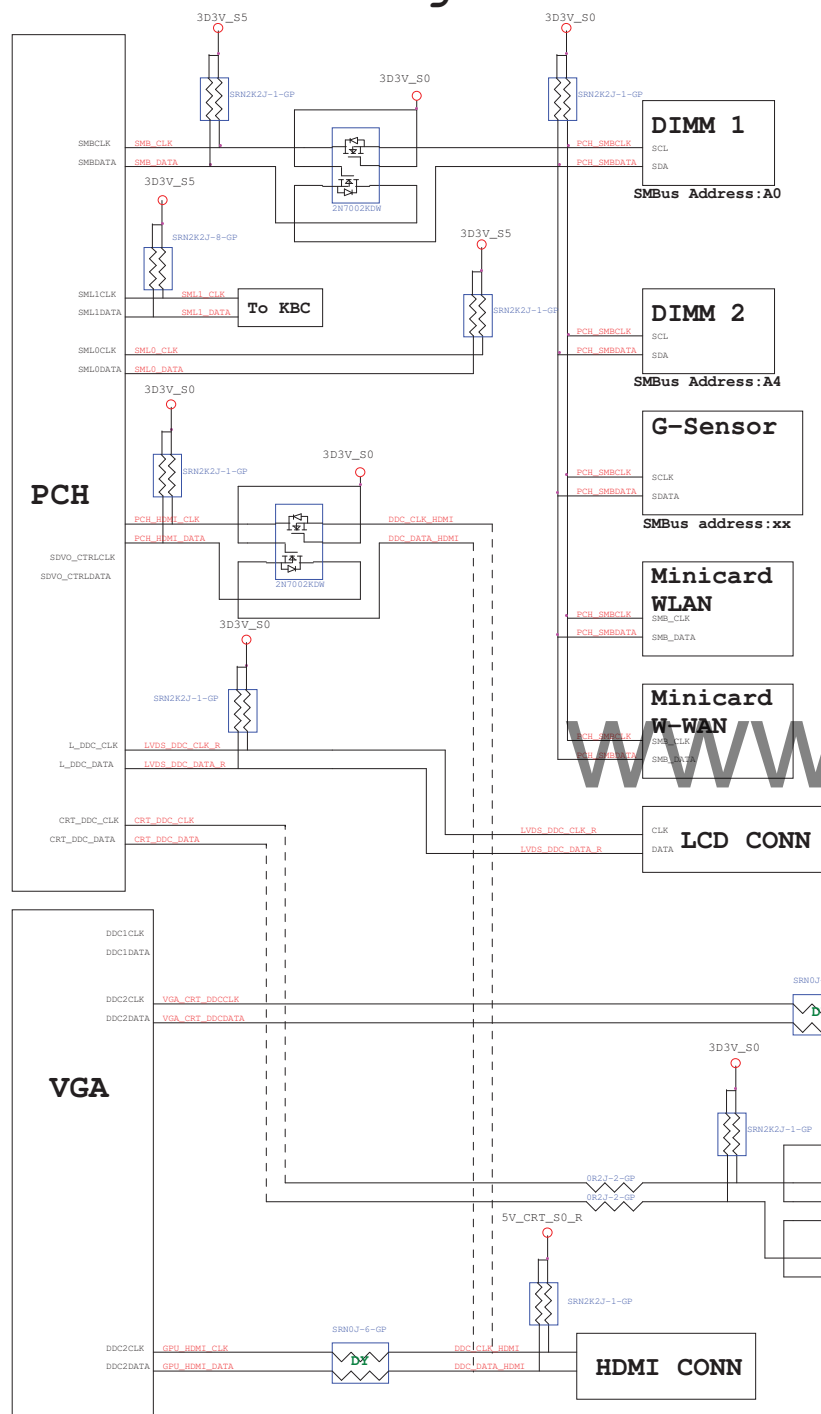
Signals and Control:

- PM_SLP_S4# (3):** Sleep signal for the system.
- PM_SLP_S3# (4):** Sleep signal for the system.
- PM_SLP_S3# (5):** Sleep signal for the system.
- PM_SLP_S3# (6):** Sleep signal for the system.
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- PM_SLP_S3# (99):** Sleep signal for the system.
- PM_SLP_S3# (100):** Sleep signal for the system.

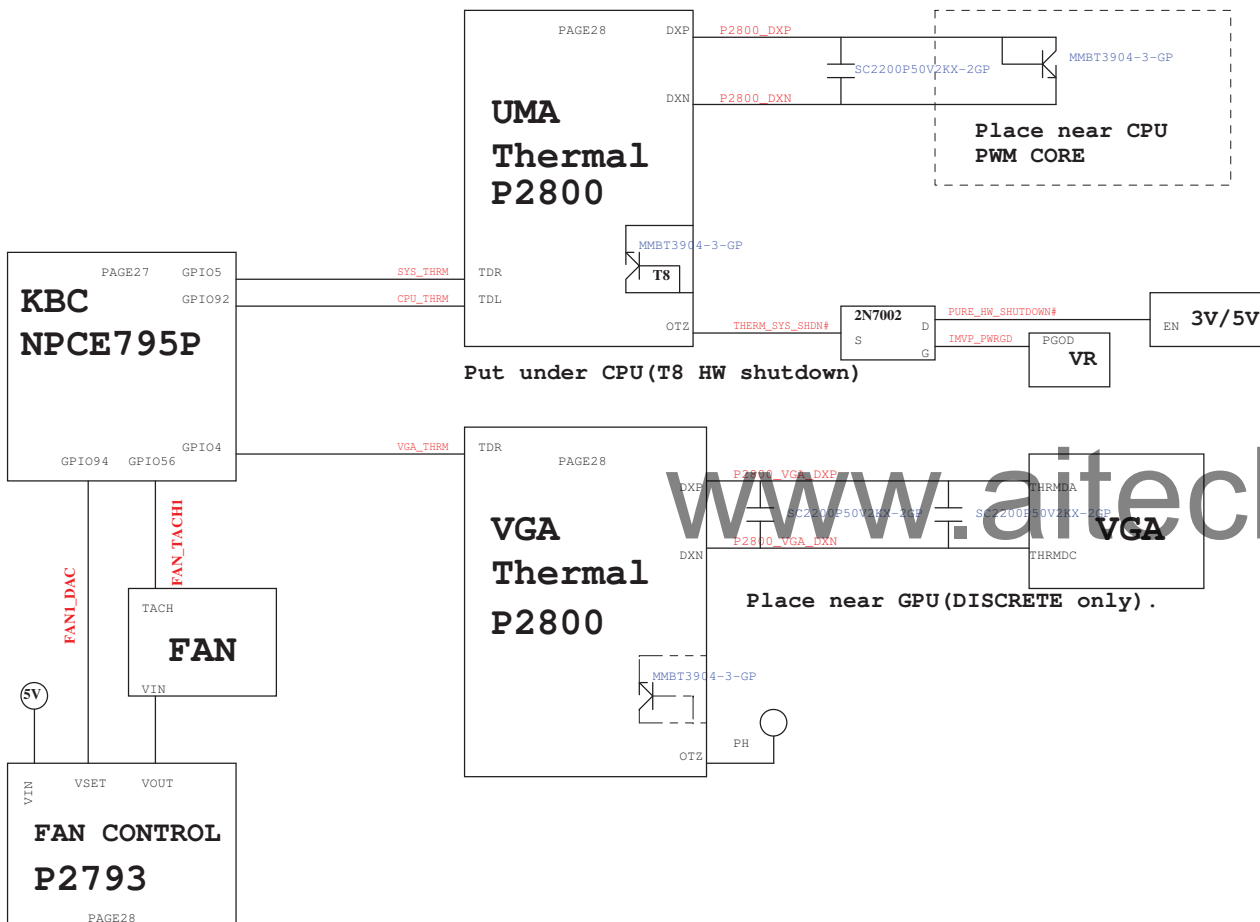
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		Wistron Corporation 21F, 88, Sec. 1, Hsien Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Power Up Sequence Diagram			
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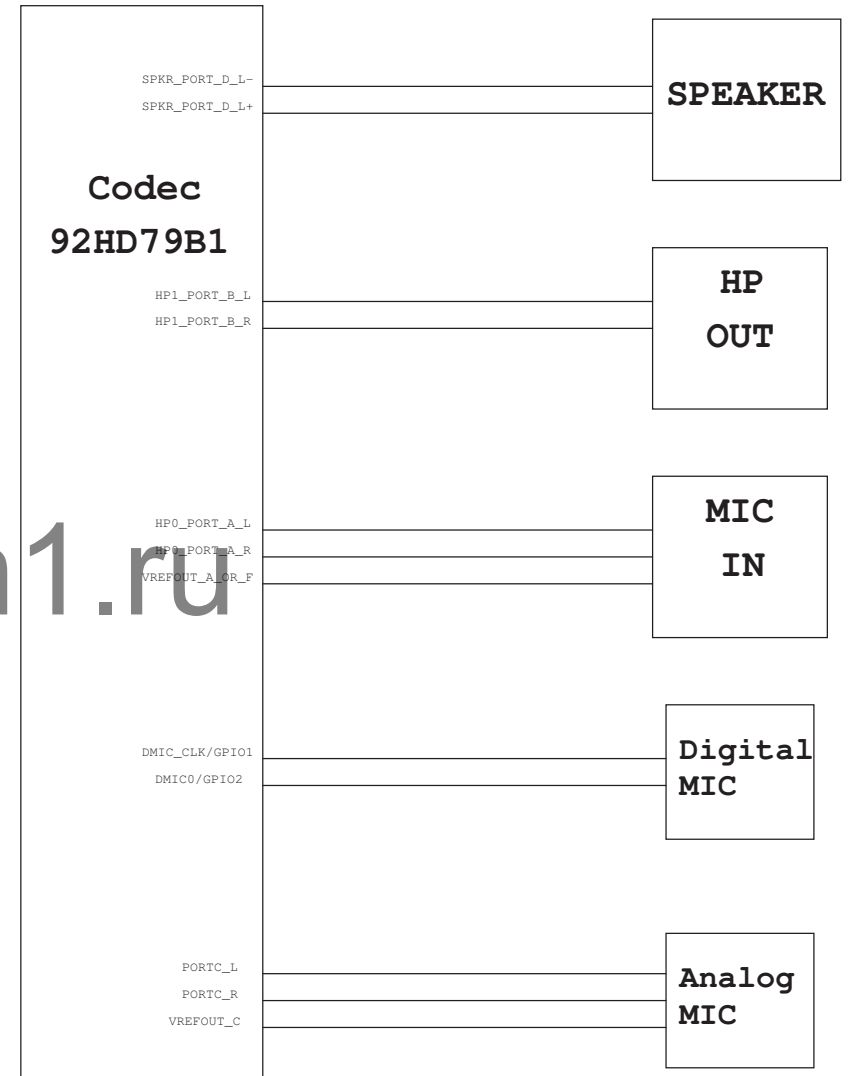
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Version	Date	Page	Function	Change Item
A00	20101222	40	Power	Power/Brian: Change PR4047 to 174k ohm from 121k ohm. Change PR4035 to 300k from 49.9k. Change PR4031 to 150k from 0 ohm. Change PR4034 to 0 ohm pad. Stuff PQ4003. Change PR4036 to 0 ohm pad. Stuff PQ4004. Change PR4037 to 76.8k ohm from 49.9k ohm. Change PR4032 to 0 ohm pad.
A00	20101222	42	Power	Power/Brian: Change PU4201 to 74.01316.F33.
A00	20101224	85	EE	Un-stuff THERMTRIP_VGA related circuit at A00 stage for fixed auto shut down issue.
A00	20101224		EE	Change all of 0ohm to short pad at X-build stage: 0402: R1404 R1405 R1503 R1504 R5010~R5012 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R3614 R3710 R8210, R8506,R8509, L8703,L8704,L8705,L8706, R8316,R8601, PR9215 0603: R5803 R5804 R8507 Parallel resistor: RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2016 RN5117,RN5112,RN5113,RN5114,RN5115
A00	20101224	93	EE	Un-stuff 1D8V_S0_VGA_PG related circuit at X-Build stage.
A00	20101224		EE	Rename PRN3901 to PN3901. Rename PTC4101~PTC4103 to PT4101~PT4103. Rename LINEOUT1 to LOUT1. Rename PWRBTN1 to PWRBT1. Rename HALLSW1 to LID1.
A00	20101224	27	EE	Change R2724 to 47K from 33K.
A00	20101224	28	EE	If stuff P2800EA1 then must stuff R2803,R2804 C2805 but if stuff P28003B0 should be un-stuff.
A00	20101224	93	EE	Change PR9311,PR9327 to short pad at X-Build.
A00	20101227	32,42,46 62,64,65 70,84~86 88	EE	Change R3210,R3211,PR4217~PR4220,PR4254;PR4605,PR4607,PR4611,PR4602;R4908,R4909,R4919,R4920,R4903,R4910,R4913~R4916R4917,R4918; R5013~R5016; R6205; R6403,R6404;R6511;R6902;R7002;R8409;R8524;R8605 ;R8812,R8830to 0R 0402 pad.
A00	20101228	93	EE	Change PR9320 to short pad at X-Build.
A00	20101228	23	EE	0402 0R pad: R2301.
A00	20101228	27,62,82	EE	VGA_THRM change to USB_PWR_EN.
A00	20101228	27	EE	Change R2756,R2763,R2766 to 0R short pad.
A00	20101228	28	EE	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at X-Build.
A00	20101229	86	EE	Change C8601 to 10uF 0805 size.
A00	20101229	71	EE	DB1 change to ZZ.00PAD.Y41(solder mask type) and keep un-stuff at X-Build stage.
A00	20101229	27,62,82	EE	Rename USB_PWR_EN to USB3_PWR_ON. Remove R6205,R620. Remove R2809 and R8210. Connect USB3_PWR_ON from KBC to IOBD1.L61.
A00	20101230	41,65,85	EE	Change PR4119 to 0R short pad. Change PR4114 to 0R short pad. Change R6406,R6405 to 0R short pad. Change PR4115 to 0R0603 short pad. Change PR4116 to 0R0603 short pad. Change R6510 to 0R 0603 pad. Change R8512 to 0R0603 short pad. Change PR4103,PR4104 to 0R0805 short pad.
A00	20101231	43	Power	Power/Brian: change PL4201 to 68.2415N.101 from 68.10110.10G.
A00	20101231	42,50,18 14,9,8	EE	Change PR4209,PR4212 to PN4201 10k array resistor. Change R5004,R5005 to RN5001 33 ohm array resistor. Merge R1804,R1806 to RN1804 22 ohm array resistor. Merge R1401,R1402 to RN1401 10k ohm array resistor. Merge R906,R907 to RN902 100 ohm array resistor. Merge R801,R802 to RN801 100 ohm array resistor.
A00	20110103	68,82	EE	Change R6801,R8201~R8203 to 1k.
A00	20110103	41	Power	Change PR4106 to 0R0603 short pad.
A00	20110104	5	EE	merge R512,R514 to RN502 1k array resistor.
A00	20110104	8	EE	Swap VCC_CORE to RN801.4 and VCCSENSE to RN801.1.
A00	20110104	9	EE	Swap VCC_GFXCORE to RN902.1 and VCC_AXG_SENSE to RN902.4.
A00	20110104	14	EE	Change RN1401 to 0R short pad.
A00	20110104	15	EE	Change R1502 to 0R0402 short pad.
A00	20110104	17	EE	Merge RN1701,RN1706 to RN1703 2.2k array resistor.
A00	20110104	22	EE	Merge RN2201,R2222,R2223 to 10k array resistor.

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Core Design

SizeA3

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A00

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